RL-TR-96-280
Final Technical Report
April 1997

MONOLITHIC, RECONFIGURABLE, PARALLEL, TWO-DIMENSIONAL, OPTICAL INTERCONNECTIONS FOR OPTICAL COMMUNICATIONS AND COMPUTING SYSTEMS

The University of New Mexico

Julian Cheng

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.

Rome Laboratory
Air Force Materiel Command
Rome, New York

This report has been reviewed by the Rome Laboratory Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RL-TR-96-280 has been reviewed and is approved for publication.

APPROVED:

PAUL L. REPAK
Project Engineer

FOR THE COMMANDER:

GARY D. BARMORE, Maj, USAF
Deputy Director
Surveillance & Photonics Directorate

If your address has changed or if you wish to be removed from the Rome Laboratory mailing list, or if the addressee is no longer employed by your organization, please notify RL/OCPC, 25 Electronic Pky, Rome, NY 13441-4515. This will assist us in maintaining a current mailing list.

Do not return copies of this report unless contractual obligations or notices on a specific document require that it be returned.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	April 1997	**FINAL, Mar 92 - Jun 96**

4. TITLE AND SUBTITLE
MONOLITHIC, RECONFIGURABLE, PARALLEL, TWO-DIMENSIONAL, OPTICAL INTERCONNECTIONS FOR OPTICAL COMMUNICATIONS AND COMPUTING SYSTEMS

5. FUNDING NUMBERS
C - F30602-92-C-0008
PE - 63726F
PR - 2863
TA - 92
WU - 46

6. AUTHOR(S)
Julian Cheng

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
The University of New Mexico
Center for High Technology Materials
125 EECE Bldg
Albuquerque NM 87131-6081

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Rome Laboratory/OCPC
25 Electronic Pky
Rome NY 13441-4515

10. SPONSORING / MONITORING AGENCY REPORT NUMBER
RL-TR-96-280

11. SUPPLEMENTARY NOTES
Rome Laboratory Project Engineer: Paul L. Repak, OCPC, (315) 330-3146

12a. DISTRIBUTION AVAILABILITY STATEMENT
APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

The development of a novel optical switching technology that uses compact, integrated optoelectronic switch arrays to provide parallel optical interconnections between electronic processing elements in a dynamically reconfigurable manner, gives rise to a very compact and very-high-information-throughput optical interconnect architecture. The technology is based on the monolithic integration of vertical-cavity surface-emitting lasers (VCSELs) with other photonic and electronic technologies, including heterojunction phototransistors (HPTs) and photothyristors (PNPNs), PIN and MSM photodiodes, and heterojunction bipolar transistors (HBTs). The integration of VCSELs with other photonic and electronic components produced novel optoelectronic devices and circuits with a host of potential applications. Combining VCSELs with heterojunction phototransistors (HPTs) and photothyristors produced high performance optical switches with alternatively latching, non-latching, or bistable switching characteristics. Latching PNPN/VCSEL switches performed programmable optical logic functions, while the non-latching HPT/VCSEL optical switches performed optical switching and spatial routing operations. Reconfigurable binary HPT/VCSEL optical switches have been designed that can spatially re-route optical data controllably to different destinations. Arrays of these switches were optically cascaded to form a multi-stage optical switching network that provided parallel, multi-point optical interconnections between electronic processors, allowing them to communicate with each other through a network of integrated optoelectronic transceivers and space-division-multiplexed optical switches at a data rate of > 500 Mb/s.

14. SUBJECT TERMS
reconfigurable optical interconnects, optical switching, computer networking, integrated optoelectronics, VCSELs

15. NUMBER OF PAGES
52

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	**UNCLASSIFIED**	**UNCLASSIFIED**	**UNLIMITED**

ABSTRACT

This program began with the objective of developing a novel optical interconnect technology that would provide parallel optical interconnections between electronic processing elements in a dynamically reconfigurable manner. Our goal was to develop a switching fabric consisting of integrated optoelectronic switch arrays that offer a very compact, very-high-information-throughput, optical interconnect architecture. The technology that we had chosen was based on the monolithic integration of vertical-cavity surface-emitting lasers (VCSELs) with other photonic and electronic technologies, including heterojunction phototransistors (HPTs) and photothyristors (PNPNs), PIN and MSM photodiodes, and heterojunction bipolar transistors (HBTs). We have played a leading role in the development of monolithic optoelectronic integrated circuit (OEIC) technology based on VCSELs, as well as advancing the state-of-the-art in VCSEL technology itself.

The integration of VCSELs with other photonic and electronic components has produced novel optical and optoelectronic devices with a host of potential applications. Combining VCSELs with heterojunction phototransistors (HPTs) and photothyristors produced several families of high performance optical switches with alternatively latching, non-latching, or bistable switching characteristics, and with varying degrees of optical gain and contrast. Non-latching optical switches integrating VCSELs and HPTs are particularly useful for optical switching and spatial routing operations.

We have developed an optical interconnect architecture and a high-speed OEIC switching technology that can provide reconfigurable interconnections between electronic processors, allowing them to communicate through a network of integrated optoelectronic transceivers and compact, monolithic, space-division-multiplexed switches that provide an optical link to other nodes and electrical access to each processor. These reconfigurable binary HPT/VCSEL switches can detect, regenerate, and spatially re-route optical data, and can be programmed by simple voltages to perform different optical routing, fan-out, and logic functions. Arrays of switches with high optical gain were optically cascaded to form a multi-stage optical switching network that provide multi-point interconnections between nodes, through which multiple data channels can be routed in parallel without intermediate optoelectronic signal conversion. The functional capabilities of this reconfigurable optical switching fabric have been demonstrated at a data rate of >500 Mb/s.

In this final report, we summarize our achievements under this Rome Labs research program, which began 1992 with the objective of developing a novel optical interconnect technology that would provide parallel optical interconnections between electronic processing elements in a dynamically reconfigurable manner. Our goal was to develop a switching fabric consisting of integrated optoelectronic switch arrays that offer a very compact, very-high-information-throughput, optical interconnect architecture. The technology that we had chosen was based on the monolithic integration of vertical-cavity surface-emitting lasers (VCSELs) with other photonic and electronic technologies, including heterojunction photo-transistors (HPTs) and photothyristors (PNPNs), PIN and MSM photodiodes, and heterojunction bipolar transistors (HBTs). During the past four and a half years, we have played a leading role in the development of monolithic optoelectronic integrated circuit (OEIC) technology based on VCSELs, as well as advancing the state-of-the-art in VCSEL technology itself, which was in a nascent phase of development at the outset of this program.

The integration of VCSELs with other photonic and electronic components has produced novel optical and optoelectronic devices with a host of potential applications. Combining VCSELs with heterojunction phototransistors (HPTs) and photothyristors produced several families of high performance optical switches with alternatively latching, non-latching, or bistable switching characteristics, and with varying degrees of optical gain and contrast. Latching switches are useful for optical data storage and for performing logic operations, and a programmable optical logic gate array can perform many complex sequential optical logic functions. Non-latching optical switches integrating VCSELs and HPTs are particularly useful for optical switching and spatial routing operations, which was the main focus of our Rome Labs program.

One of the main applications of a reconfigurable optical interconnect technology is to link many electronic processors together to form an interactive network with a parallel processing capability. This calls for dynamically reconfigurable interconnections that can route a large volume of digital data between many different computer processors and shared memory facilities, allowing them to communicate simultaneously in real time. We have developed a optical multi-access interconnect architecture and a high-speed OEIC switching technology that provide reconfigurable interconnections between electronic processors, allowing them to communicate through a network of integrated optoelectronic transceivers and compact, monolithic, space-division-multiplexed switches that provide an optical link to other nodes and electrical access to each processor.

The integrated optical routing switch arrays that we have developed can route many input optical data channels simultaneously to different optical output ports in a dynamically controllable manner. These reconfigurable binary HPT/VCSEL switches can detect, regenerate, and spatially re-route optical data, and can be programmed by simple voltages to perform different optical routing, fan-out, and logic functions. Arrays

of switches with high optical gain were optically cascaded to form a multi-stage optical switching network that provide multi-point interconnections between nodes, through which multiple data channels can be routed in parallel without intermediate optoelectronic signal conversion. This programmable optical interconnect architecture can be used as a parallel, spatially-multiplexed, optical packet-switch. Most of the required functional capabilities of this reconfigurable optical switching fabric have been demonstrated at a data rate of >500 Mb/s, which exceeded the B-ISDN rate of 155 Mb/s, and the 622Mb/s target is easily within reach.

Optical switching can also be expanded beyond its spatially-multiplexed context into the temporal or spectral domain, using VCSELs in a time-division-multiplexed or wavelength-division-multiplexed format. Using an array of VCSELs or other lasers in a novel electrical gain-switching scheme, we demonstrated the generation of directly-modulated, time-compressed, and time-delayed optical pulses in a single operation, plus thye ability to perform time-slot-interchange (temporal switching) operations. Switching has been achieved at a data rate of >1Gb/s per channel, with a aggregate time-multiplexed data capacity of >10 Gb/s.

I. Discussion of this Program and a Summary of its Accomplishments:

For short-distance data networking applications, there is a growing need for parallel optical links and high-speed, multiple-access buses to alleviate the input/output bottleneck in data communication. In the past, the insertion of photonic technology into the data communication market has occurred only in the form of simple point-to-point optical data links that required no reconfiguration. But as computers improve in speed and processing capacity, and are increasingly being linked together in to form interactive, shared facility networks, the increased demand for data communication requires new interconnect paradigms that provide real-time, parallel data transfer at increasingly higher data rates. The focus will shift from single-access, point-to-point optical links towards more flexible multiple-access networks that can route a vast amount of information simultaneously and interchangeably between a large number of nodes via rapidly reconfigurable interconnections. This involves not only the transmission, but also the switching and routing of optical data. In this program, we have designed a new, dynamically reconfigurable optical interconnect technology that addresses the requirements of future computer networks, and we have developed an enabling switching technology based on the integration of vertical-cavity surface-emitting lasers (VCSELs) with other photonic and electronic component technologies.

Traditionally, switching can be performed at lower frequencies in the electronic domain through electronic crossbars and bus switches, which are limited in both speed (< 100 Mb/s) and in switching matrix size. As the processor speed and data throughput both continue to increase, it will become increasingly difficult to produce the switching networks needed for routing a large number of data channels. With the processor speed already surpassing 250 MHz, and the data width rapidly moving towards 64 bits and beyond, parallel and high-speed data buses are needed to support the peak

processor performance without intermediate multiplexing and demultiplexing (MUX/DEMUX) operations. But at higher speeds and/or larger transmission distances, the communication between the nodes becomes increasingly dominated by latency, timing skew, and power dissipation, which can be reduced by replacing the electrical interconnection with an optical fabric. This provided the motivation for our research in photonic switching networks that would allow many parallel data channels to be routed simultaneously in the optical domain. Since data is transmitted between distant nodes in an optical format, there is electrical isolation between successive stages.

Dynamically reconfigurable optical switching networks are useful for a variety of applications in parallel optical processing. They have important applications in future high speed computer systems, where large numbers of individual processors will be linked together to form interactive, shared-facility networks with the enhanced computational power of a supercomputer. They may be used to interconnect a large number of boards in the backplane of a parallel multi-processor network, which can be programmed rapidly in real time to perform multiple tasks in parallel. Alternatively, they may also be used to interconnect a network of interactive computers that are distributed across distant spatial locations, where the larger distances and higher speeds involved make an optical link imperative. Individual processors must have multiple access to the optical network in order to facilitate the simultaneous communication between many different processors. The flexible, monolithic optoelectronic technology that we have developed can optically interconnect a network of local or distributed computer processors. These high-speed electronic processors may reside as multi-chip-modules (MCMs) on different boards, each of which contains an array of optoelectronic routing switches that provide access to an optical network, whose total data capacity may reach tens of Gb/s.

Since data communication generally tends to be bursty in nature, the optical interconnect architecture must be able to dynamically re-route many sources of packetized optical data simultaneously through different channels. In addition to being a densely parallel optical link, reconfigurability is needed to facilitate the intelligent routing of data packets. These packets may be transmitted through an interactive optical network with a local self-routing capability, or the connections may be programmed in a centralized fashion by a host computer.

During the course of this program, much work was also done to improve the performance of VCSEL technology, which had provided us with an early lead in achieving many different high performance optoelectronic device technologies based on VCSELs. These included several families of optical switches with alternatively latching, non-latching, or bistable characteristics (1991), monolithic optical logic gates and logic families (1992), reconfigurable optical routing switches (1993), programmable optical logic gates (1994), high-speed optical transceivers (1995), an optically cascaded multi-stage switching fabric (1995), and a programmable optical logic gate array (1995).

In the first phase of this program, we had developed the enabling technology for a high-speed optoelectronic switching fabric. The technology consisted of monolithic arrays of surface-normal binary optical switches based on the monolithic integration of heterojunction phototransistors (HPTs) with vertical-cavity surface-emitting lasers (VCSELs). Each switch node contains a HPT, which provided an optical input port, optoelectronic signal conversion, and electronic gain, and a VCSEL that provided the optical output. The HPT/VCSEL switch is a regenerative optical device that amplifies the input optical signal to produce a larger optical output. By interconnecting pairs of these switching nodes in a specific manner, optical bypass-exchange switching operation was achieved. The input optical data channels were routed in either a straight-through (bypass) or crossed-over (exchange) mode in response to simple routing control voltages. Reconfiguration occurred at a speed approaching the switching speed of an HPT/VCSEL switch, although that is not necessary for the routing of optical data packets. Each binary switch thus provides an optical-to-optical interface for optical communication between processors, as well as O/E and E/O interfaces to electronics, and it also performs the optical routing functions. A large number of HPT/VCSEL switches can be readily integrated on a single chip, which provides a large and compact routing matrix with relatively short electrical signal path lengths. At the system level, we have used these reconfigurable routing switch arrays to demonstrate a novel and dynamically reconfigurable, multi-stage optical interconnection network.

Our approach to a reconfigurable photonic switching network is based on space-division multiplexing (SDM), which allows a large number of optical data channels to be routed to different destinations in parallel using two dimensional optical switch arrays. The usefulness of this optical interconnect is greatly enhanced by the fact that all the routing paths are dynamically reconfigurable, and the network is flexible enough to permit one-to-one, broadcast, or multi-cast operation. We will summarize our accomplishments for this program in detail below.

2. Detailed Summary of Program Achievements:

2.1. Development of High-Performance VCSEL Technology:

VCSELs are ideally suited for parallel optical interconnect applications since they are readily integrated into dense, two-dimensional arrays to provide a compact, parallel, surface-nomal architecture. The VCSEL provides a high speed optical source with good optical beam quality, high output power, low power dissipation, good thermal stability, stable current-voltage characteristics, and a very wide operating temperature range. Much of our work on switching requires the achievement of high performance VCSELs, and a significant amount of work was done to improve their characteristics, including their modulation speed (~10 GHz measured bandwidth, 45 Ghz intrinsic), their thermal stability (<3 dB variation in threshold over a temperature range 150°C wide), and more importantly for switching, their slope efficiency (45%), power conversion efficiency (22%) and their integrability with other technologies (VCSELs on both p-type

and n-type, as well as on semi-insulating substrates). We have fabricated two types of VCSELs (figure 1), whose active areas are defined by proton implantation (upper) and oxide confinement (lower), respectively. The typical characteristics a of 16 μm diameter proton-implanted device are shown in Fig. 2.

Our first major contribution to VCSEL technology was to demonstrate that the VCSEL's electrical characteristics can be greatly improved by the continuous compositional grading and selective doping of the heterointerfaces by using MOCVD. This reduced the barrier resistivity to a level approaching that of barrier-free bulk transport, and for the first time, we had dropped the operating voltages of VCSELs from 5-10 V down to 2 V, and the series resistance from 300 Ω to less than 50 Ω (1991-92). It would be two years before other group would achieve these results. We also showed that the temperature dependent behavior of VCSELs is strongly limited by the roll-over of its lasing characteristics resulting from the thermally-induced de-tuning of the lasing mode with respect to the gain peak (1993), which curtailed its temperature range of operation. By aligning the cavity mode to the gain peak, power dissipation is reduced, allowing the resulting VCSELs to to achieve very stable current-voltage characteristics and stable lasing operation over a wider range of temperature (100K to 580K pulsed, 100K to 410K cw). This relaxed the need for thermally-compensated drive ciruits and alleviated the thermal management issues. VCSELs with lasing wavelength variations of less than 1% across a 2" wafer was also achieved.

From our experimental modeling work on VCSELs, we clarified the intrinsic and extrinsic effects that governed their modulation response (intrinsic $f_{max} \cong 44$ Ghz). We have also carried out optical fiber transmission experiments at a data rate of up to 1 Gb/s, using a VCSEL-based transmitter and both single-mode and multi-mode fibers. Figure 3 shows a wide open eye diagram at a signal level of -20 dBm, with a bit-error rate of better than 10^{-13} for the latter, and about 10^{-10} for the former, which was limited by dispersion and mode-selective loss. We were also the first to achieve an inverted VCSEL structure grown on a p-type GaAs substrate (1993), which is advantageous from the perspective of achieving faster electronic drive circuits (by using silicon npn-transistors) or for optoelectronic integration).

2.2. A Spatially-Multiplexed, Dynamically Reconfigurable Optical Interconnect Architecture

An optically regenerative, surface-normal photonic switch that provides optical amplification as well as two-dimensional access could result in a compact and more densely-packed monolithic architecture. By optically cascading these switching arrays, a very compact, multi-stage, optical interconnection network can be realized. Figure 4 shows a reconfigurable optical architecture that illustrates many of the functions that may be required in a highly-parallel optical processor, in which parallelism takes on the form of two-dimensional arrays. Different array technologies are needed to perform the various functions in the optical domain, including: optical data generation, amplification, and detection, optical logic or other digital signal processing functions, optical data

storage. But most importantly, dynamical reconfiguration of the optical data paths is needed to allow these arrays to perform different functions using the same hardware, thereby providing the processor with the kind of programmability that is similar to an electronic programmable logic gate array. When the emphasis is on reconfiguration, the array processor functions as a programmable optical routing switch. When logic is emphasized, however, the processor becomes a programmable optical computer or digital signal processor. Optical logic and the primary optical switching functions were the goals of a related research program funded by AFOSR. In this Rome Labs program, our emphasis is on the data routing functions and on their applications to reconfigurable optical interconnects, such as a switchable optical backplane or a reconfigurable multi-processor network.

An important application for this optical switching fabric is that of a reconfigurable optical network interconnecting a large number of electronic processors consisting of mutli-chip modules (MCMs) residing on the same board or on different boards (figure 5). Electronic processors currently communicate with processors on other boards via parallel electronic data buses. With increasing processing speeds or larger transmission distances, the communication between boards becomes increasingly dominated by latency, timing skew, and power dissipation, which can be reduced by replacing the electrical interconnection with an optical one, using fiber or free space as the transmission medium. In addition to providing optical interconnections between successive processing stages, the switching fabric also provides optical-to-electronic (O/E and E/O) interfaces to VLSI electronics. At each end of the optical link is an electrical-to optical (E/O) or optical-to-electrical (O/E) interface that converts data between its electrical and optical formats. For simple parallel optical interconnects, these interfaces mostly consist of optical transmitter and receiver arrays that provided fixed paths between selected processors. As larger numbers of high-speed computer processors are linked together to form interactive networks with a parallel processing capability, there is a need for real-time, parallel communication between different processors at increasingly higher data rates. This requires an optical interconnection network that provides dynamically reconfigurable connections between nodes, and which can support a larger switching matrix size while providing higher speed and optical isolation between stages.

Our approach to a large-scale multi-processor interconnect is based on the dynamic reconfiguration of a multi-stage, multi-path, space-division-multipled optical routing network (figure 6). Space-division-multiple access (SDMA) networks can provide a very large spatial bandwidth since large, compact switching matrices can be achieved by optoelectronic integration, and many parallel channels can be routed simultaneously through space. By arranging the network in the form of a closed ring, any node can be interconnected to another by selecting a routing path through the switching fabric with a small number of intermediate hops. Figure 6 shows a *dynamically reconfigurable optical interconnection architecture* for optically linking electronic processors together and routing data through parallel optical channels. A network of optoelectronic switches

provide optical links between nodes and electrical access (an electrical ⇔ optical interface) to each processor. Each node must be able to transmit or receive optical data, or to re-route it optically to the next stage (routing or optical bypass mode). The received optical data (P_{in}) is converted into electrical data (E_{out}), which is either *dropped* at that node, or is *regenerated optically* and routed to the next stage (P_{out}). The switch must also accept electrical input data (E_{in}) from a local processor and convert it to an optical format (P_{out}) for transmission. To perform the transceiver functions, each switch must provide an optical source and photodetector, as well as their drive circuitry and the switching functions, and it must be able to convert digital data between various electrical and optical input/output formats.

Figure 5a shows a 4-stage Banyan network that provides complete connectivity between 64 processors distributed into 4 clusters, each with 16 nodes. Each node can transmit data to other nodes through one or more intermediate hops, using optical signal paths that can be individually programmed. The signals are optically cascaded between stages until they reach their destinations, where they are converted back into electrical data. The switching fabric consists of 4 monolithic arrays of optoelectronic switches, each with 16 optical input and output ports, and each switch node is capable of performing either the optical switching or optoelectronic signal conversion functions. The example of a 1x8 linear HPT/VCSEL switch array is shown schematically in figure 5b, and the optical switching and optoelectronic conversion functions of a 2x2 multiprocessor interconnection network are illustrated in figure 5c. Each node is connected to a shared optical transmission medium (free space or fiber), with which it interacts by transmitting, receiving, or optically bypassing optical data. The compact monolithic switch arrays contain very short electrical routing paths, while their optical outputs can be projected across signficant physical distances.

Figure 5c also shows a simplified two-stage optical interconnection network that illustrates the communication of data between four N-bit processors residing on two different boards. Each board also contains one stage of a 2x2 optoelectronic switching matrix, with two nodes per stage, each of which is electrically connected to a processor (only one bit is shown). Each switch node can be activated by either an optical or electrical input, and produces either an optical or electrical output. Each node can be modulated, either by an optical input from another node or by an electrical input from its associated processor, to produce a current modulation that is spatially routed to one or more nodes within the switch array, where it produces both a modulated electrical signal that is sent to the corresponding processor and a regenerated optical output that is optically transmitted to the next stage. The internal routing paths within each array can be reconfigured by setting the control voltages. Parallel optical data channels propagate between boards through free space or through a weakly-guided medium, and are routed to other nodes in successive stages under electronic routing control. Local or centralized routing control can be used, and both packet and circuit switching are possible.

2.3. The Achievement of a Reconfigurable Switching Technology

2.3.a. Optical Switches Based on the Integration of VCSELS with HPTs and PNPNs

The integration of VCSELs with other photonic and electronic components produced novel optical and optoelectronic devices with a host of potential applications. Integrating VCSELs with heterojunction phototransistors (HPTs) and photothyristors (figure 7) produced several families of high performance optical switches with alternatively latching, non-latching, or bistable switching characteristics (figure 8). These switches possess greatly varying degrees of optical gain and contrast, as well as an adjustable switching threshold. Latching switches are useful for optical data storage and for performing optical logic operations, and a programmable optical logic gate array has been made that can perform many complex sequential optical logic functions, which we have demonstrated under a related Air Force contract. Non-latching optical switches integrating VCSELs and HPTs form the technology base for the optical switching and spatial routing operations that are the concern of this RADC program.

2.3.b. Reconfigurable Binary Optical Routing Switches

Reconfigurable spatial routing of optical data packets can be achieved by using a simple, binary optical bypass-exchange switch (figure 9) consisting of a two-segment HPT, each of which is connected to a different VCSEL. The VCSEL and HPT epilayers are monolithically integrated on the same GaAs substrate (figure 9c). By segmenting the HPT into two contiguous but electrically-isolated segments that share a common optical input, and connecting each segment to a different VCSEL output port, reconfigurable spatial routing of the input optical data can be achieved by independently controlling the bias voltages of each HPT/VCSEL pair. Figure 9(a) shows the design and optical routing functions of a binary 1x2 switch. By controlling the voltages V_1 and V_2, packets of optical data impinging on the HPT generate an amplified photocurrents I_c that modulates the VCSELs independently to produce optically regenerated outputs that emerge from either, neither, or both (fan-out of 2) of the output ports. Electrical routing within each stage is limited to very short distances within a compact two-dimensional array of switch nodes. The routing paths and optical fan-out are controlled by the voltages V_1 and V_2, as demonstrated experimentally in Fig. 10. Arrays of 1x2 switches form each stage of the multi-stage shuffle network that is depicted in figure 7, and all the connections can be dynamically reconfigured using the routing control voltages.

The 2x2 optical bypass-exchange switch (figure 9b) consists of two 1x2 switch nodes pairing the same two input and output channels. Arrays of 2x2 switches may be used to implement routing networks with a Banyan topology. Routing is controlled by two pairs of voltages - (V_1, V_2) and (V_2', V_1') - which select the bypass or exchange mode of the switch. These optical switching functions are experimentally demonstrated in figure 11. As the routing control voltages are toggled between the two inner and

outer switch connections, the optically regenerated pulses of the two input data channels emerge alternately from the same or opposite output ports (VCSELs).

In 1993, both 1x2 (figure 10) and 2x2 (figure 11) versions of this HPT/VCSEL switch were used to demonstrate programmable spatial routing and optical fan-out at a data rate of 20 Mb/s. More recently (1995), the optical switching speed was increased by an order of magnitude to 200 Mb/s using an improved switch design.

The reconfigurable binary HPT/VCSEL switches can detect, regenerate, and spatially re-route optical data in a programmable manner. The multi-functional capability of these binary switches is illustrated in Fig. 12, which shows that a single array of these switches can be programmed by simple voltages to perform different optical routing, fan-out, and logic functions. Arrays of these switches can be cascaded to form a multi-stage optical switching network that routes data through parallel optical channels to provide multi-point interconnections between nodes. These interconnections can be dynamically reconfigured, thus providing a useful platform for a parallel, spatially-multiplexed packet switch or a multi-processor interconnect.

2.3.c. Optoelectronic Integration of VCSELS with HBT Technology

The integration of VCSELs with high speed electronics is driven by: 1) the desire to combine the optical source array and its driver circuits into a single technology, and 2) to provide a simple optoelectronic interface for VCSEL-based photonic switching networks. Before the electronic processing elements can communicate with each other through parallel optical channels, an optoelectronic interface is needed to effect electrical $\Leftrightarrow$ optical signal conversion. This interface must perform the functions of an optical transceiver, allowing the switch to communicate with a processor or its electronic control functions. The integration of VCSELs with heterojunction bipolar transistor (HBT) technology is favored by the compatibility of their epitaxial structures, operating current densities, physical sizes, and modulation speeds.

The simplest VCSEL drive circuit is an HBT/VCSEL optoelectronic switch in an emitter-follower configuration, which is mandated by the common n-substrate contact of the VCSELs. A common-emitter configuration would be more suitable, and allows more flexible connections to be made among devices, but this requires that the VCSELs be grown on a p-type or a semi-insulating substrate. In 1992, we achieved the first monolithic optoelectronic switch integrating a VCSEL with a GaAs/AlGaAs HBT (figure 13), with a high current gain (β~500) and a large electrical-to-optical conversion efficiency (150 mW/mA), but high speed switching performance was limited to a small-signal bandwidth of $\approx$100 Mhz ($\approx$50 Mb/s).

Figure 14 shows the small-signal, (a) electrical and (b) optical modulation response of an integrated HBT/VCSEL switch with a 10x10μm^2 emitter area and a VCSEL active area diameter of 20μm. The dc current gain of this device is β=31 at a collector current of I_C=10mA. At this bias level, the HBT saturates at 1.5V, while the VCSEL threshold voltage is 2.1V, and switching can be effected with a collector bias of

less than 5V. The relative small-signal response of I_c to a voltage modulation applied to the base is shown in Fig. 14c, which shows the forward transmission coefficient S_{21}, and the current gain h_{21}. The HBT has a unity-gain bandwidth of 500MHz, with a corresponding time constant τ=0.32ns. Figure 14d shows the small-signal electrical-to-optical modulation response of the switch at different values of bias current, which has the typical resonant frequency response of a diode laser modulated above threshold, modified by the transconductance of the follower circuit. The modulation response saturates at a bandwidth of f_{max}~4GHz.

Figure 14b shows the eye diagrams of this HBT/VCSEL switch under 500Mb/s, large-signal pseudorandom data modulation. The upper trace represents the modulated light output of the VCSEL, while the lower trace shows the modulated collector current I_c. The modulated electrical pulses have a 10%-90% transition time (~2.2τ) of 0.6ns, and shows no significant pulse narrowing due to a turn-on delay when the switch is pre-biased above the lasing threshold. A much higher modulation bandwidth was later achieved by using self-aligned HBT technology and improved processing (figure 15). The same epitaxial structure can also be used for the integration of VCSELs with more complex HBT electronic logic and interface circuits, or with phototransistors to perform the optical switching functions. Arrays of such switches form a compact optoelectronic interface for a parallel optical data link.

2.3.d. Integrated 3-Terminal HPT/VCSEL Switch with an Optoelectronic Interface

High performance optical and optoelectronic switches with high gain and contrast, and moderately low optical switching energies have been made by integrating the VCSEL with an HPT. As we have seen (figures 10-12) these switches have been combined into binary configurations to perform different spatial routing functions, such as the bypass and exchange of optical signals, under simple voltage control, but an electrical interface was lacking. Using a three-terminal HPT/VCSEL optical switching technology, we have shown that the functions of the HPT and the HBT can be combined in a single switch (figure 16), thereby integrating both the optical switching and optoelectronic signal conversion (interface) functions. These *multi-functional* switches can perform different combinations of electrical and optical switching at high data rates, and it can combine electrical and optical data packets into a common format.

By replacing each of the two-terminal HPTs in a binary optical routing switch with a three-terminal(3T)-HPT, and adding the electrical input and output ports, these spatial routing switches can perform the simplified transceiver functions. Figure 16(a,c) shows an integrated switch consisting of a three-terminal heterojunction phototransistor and a VCSEL. The switch can be activated by either an optical signal (P_{in}) from another node or by the electrical input (E_{in}) from a local processor, producing a switched optical output (P_{out}) from the VCSEL that is transmitted to the next node, as well as a modulated collector current (I_c) and an output voltage (E_{out}) that is coupled to an electronic processor in the cluster (figure 16b). The phototransistor base terminal

serves as an electrical input port for both data and prebias, and the operating characteristics of the switch can be adjusted using the latter. For example, the switch can be prebiased near the lasing threshold of the VCSEL to minimize the optical power needed to effect switching. Each node can either receive or transmit optical data, or optically re-route it to other nodes in the optical switching network. The optical response of P_{out} to a voltage E_{in} applied to the base of the HPT represents the transmitter function, while the response of E_{out} to an optical input P_{in} incident on the HPT represents the receiver function. The production of an *optically switched* and *optically regenerated* output P_{out} in response to P_{in} represents the optical bypass or routing function.

The experimental HPT/VCSEL switch contains a VCSEL with a 20 μm active area and a lasing threshold of 5.2 mA, and a 3T- HPT with a differential current gain of of β~50. The optical input P_{in} illuminates an area lying between the emitter and base contacts (figure 16c), and the quantum efficiency of the HPT is ≈65%. The various switching functions are demonstrated experimentally using a combination of optical and electrical inputs, and the results are shown in Fig. 16d. Two different data patterns modulate the optical and electrical inputs to the HPT during alternate, non-overlapping time intervals. The optical input P_{in} is incident on the base-collector junction of the HPT, while the electrical data E_{in} directly modulates the base of the HPT, each at a data rate of 200 Mb/s. The switch converted the electrical and optical input data packets into switched optical and electrical outputs, which were combined into a single data stream. The first two traces in Fig. 16d show the modulated collector current I_c in the presence of *only* the electrical (trace 1) or optical (trace 2) input data. Traces 3 and 4 show the modulated electrical output (I_c) and optical output (P_{out}) when the optical and electrical input data are both present, which contain replicas of both the optical and electrical inputs, thus showing the conversion of P_{in} and E_{in} into a switched optical or electrical format. Trace 3 demonstrates electrical switching and optoelectronic data conversion (receiver function), while trace 4 demonstrates optical switching and optoelectronic data conversion (transmitter function). Electrical input data E_{in} likewise produces a modulated output current and an optical output.

The large-signal modulation characteristics of the switch are depicted in Figure 16e. The eye-diagrams represent the optical response P_{out} (lower traces) and the electrical response E_{out} (upper traces) of the switch to large-signal modulation by pseudorandom optical data P_{in} (left) and electrical data E_{in} (right) at 200 Mb/s. The 10%-90% rise time of each pulse is 0.8 ns. Integrated HBT/VCSEL driver circuits with a data rate of ~1 Gb/s appear to be within reach.

2.3.e. High-Speed Optical Switching and Routing using a new Array Design:

In order to improve the performance of the binary optical switch based on the 3T-HPT design, the switching fabric was redesigned using linear arrays of individually-addressable binary HBT/PIN/VCSEL switches integrating HBTs, p-i-n photodiodes, and VCSELs. Separating the 3T-HPT into two different entities - a p-i-n photodiode (PIN)

for photodetection and a heterojunction bipolar transistor (HBT) for gain - allows each component to be individually optimized to achieve higher gain and a higher switching speed. In the new switch design (figure 17a,b,c) each node contains its own independently-addressable electrical input terminal. In addition, the input ports were re-designed so that the PIN pairs have an improved response time and a higher optical coupling efficiency. To improve switching speed, the HBTs have also been redesigned to have a smaller base-emitter junction and a lower base resistance. Arrays of 1x4 and 1x8 switches were fabricated and were used in parallel optical switching experiments. A cascadable binary optical routing switch with improved switching performance was thus realized.

High-speed electrical and optical switching, as well as the reconfigurable routing of optical signals, have been demonstrated at high speed (400-500 Mb/s), with an high optical gain of 7.5 dB, which is essential for cascaded switching operation. The HBTs used in these experiments have a dc current gain of 90, a 3-dB modulation bandwidth of 550 MHz, a rise-time (10%-90%) of 630 ps. The VCSELs has a high slope efficiency of 35%. The switches were pre-biased near the VCSELs' lasing threshold to minimize the turn-on delay.

Figure 17(d) demonstrates the conversion of a large-amplitude electrical input signal into a switched optical output. The 400 Mb/s NRZ electrical input data is applied to the base of the HBT. Figure 17(e) demonstrates the optical-to-optical switching performance of the binary switch. The input optical data impinged upon the segmented PIN pair, producing amplified photocurrent pulses that modulate the VCSEL from below threshold to an optical output level of ~1 mW. Figure 17(f) demonstrates optical routing and fan-out using the binary optical switch. The same optical input signal was coupled equally into the PIN pair, with the switch pre-biased near lasing threshold. When a bias voltage was applied to the collector of each PIN/HBT/VCSEL circuit, a single optical input signal was routed to each of the two optical output ports, modulating each VCSEL at a data rate of 500 Mb/s. Biasing only one of the circuits results in routing of the optical data to one output port or the other.

In order to optically cascade these switches in a multi-stage routing or interconnection network, each switch must possess sufficient optical gain to compensate for the optical losses incurred in coupling and transmission. The optical gain depends on the optical coupling efficiency (~18%), the PIN quantum efficiency (39%), the current gain of the HBT (90), and the slope efficiency of the VCSEL (35%). An optical gain of 7.5 dB was achieved using these switches. An improved version of the HBT/PIN/VCSEL switch based on a common p-substrate configuration is shown in figure 18.

2.3.f. Optically-Cascaded Multi-Stage Switching Operation and Reconfigurable Multi-Point Optical Interconnects:

Reconfigurable routing between a large number of node can be achieved using a mutli-stage optical routing network in which each stage contains an array of binary optical routing switches (fig. 19) that provided multi-point optical interconnections between nodes. Each node can be routed optically to any other node by selecting a path through the switching fabric using a small number of intermediate hops. Arrays of binary optical routing switches have been made by integrating VCSELs with HBTs and photodetectors (PINs) in either a monolithic or hybrid format. Each node contains a pair of PIN/HBT/VCSEL switches, whose closely spaced PINs form a single optical input port, while their VCSELs provide two spatially separated optical output ports. An optical signal incident upon the PIN pair switches on one or both VCSELs according to the routing control voltage applied to each switch. Each switch node can transmit or receive optical data, or to re-route it optically to other nodes.

We demonstrated the *reconfigurable, optically-cascaded, multi-stage switching operation of binary optical switch* arrays consisiting of PINs and HBTs integrated with VCSELs. The input nodes (pairs of PINs and HBTs) and output nodes (VCSELs) were monolithically integrated on two separate chips in order to individually optimize their characteristics and to achieve a large optical gain. When the binary optical switch can achieve a sufficient optical gain, the output of the first switch stage can be used to effect switching of the next stage, thus achieving optically cascaded switching operation. For the PIN/HBT/VCSEL switches usd in this demonstration, the dc current gain of the HBT is ~150, the external quantum efficiency of the PIN (including partition) is ~25%, and the external slope efficiency of the VCSEL is ~ 35%, giving an estimated optical gain of ~10-20.

Three linear binary optical switch arrays were used to demonstrate optically-cascaded switching operation (figure 19). The experimental configuration used to demonstrate optically-cascaded switching operation is shown in figure 20. An electrical input was applied to a node (figure 21a,b,c) in the first switch array to generate an optical output P_o, which is routed to another output port within the first array. The optical signal P_o then impinges on a switch node in 2, and produces a switched optical output P_1 with a net optical gain. By controlling the bias or routing control voltages, the switched signal P_1 can emerge as optical outputs from one or two VCSELs. This P_1 in turn impinges on another binary switch in stage 3 to produce optical output P_2 , again with an optical gain. Figures 21(d) and 21(e) show the electrical characteristics of the HBT and the optical characteristics of the VCSEL, respectively, while figure 21(f) shows the dc optical transfer characteristics of stage 2 (P_1 as a function of P_0) and stage 3 (P_2 as a function of P_1), respectively. Also shown are their derivatives, which represent the differential optical gain as a function of the input optical power for each stage. The optical gain of stage 2 has a peak value of ~18, while stage 3 has a peak value of ~4, which was due to variations in processing. The optical output power P_2 of the cascaded two-stage switching system, and the composite differential optical gain, dP_2/dP_o, are shown as a function of the input P_o in figure 21(f). The overall dc optical gain of the cascaded switches has a peak value of ~50.

The optical gain of these two stages of binary optical switches in cascaded operation have also been measured under ac modulation. At an input power level of P_1=20 μW and at a data rate of 50 Mb/s, the differential ac optical gain is $dP_1/dP_o \sim 4$ for the first stage, and $dP_2/dP_1 \sim 2$ for the second stage, giving an overall cascaded ac optical gain of $dP_2/dP_o \sim 8$.

2.3.h. Transceiver Characteristics of a PIN/HBT/VCSEL Switch and Transmission Characteristics through Optical fibers:

We have evaluated the transmission characteristics of VCSEL-based optical links, as well as the performance of the PIN/HBT/VCSEL routing switch as optical transceivers in fiber transmission experiments. For the former, high-performance VCSELs were directly modulated at a data rate of up to 1 Gb/s, using pseudorandom electrical data in a non-return-to-zero (NRZ) format, and the optical output is coupled into a single-mode or multi-mode silica fiber, respectively, with a coupling efficiency of >85% in each case. The transmission characteristics have been measured for fibers of varying lengths, ranging from 0.5 m to 1 km. A PIN photodiode and a transimpedance amplifier with a -3 dB bandwidth of 1.5 GHz was used for the receiver. Pseudorandom optical data was successfully transmitted through 1 km of multi-mode fiber at a data rate of 1 Gb/s, with a bit-error-rate of better than 10^{-13}. However, in the single-mode case, evidence of dispersion can be seen after 1 km at 650 Mb/s, and more importantly, an error floor was observed below BER=10^{-10} as a result of mode-selective loss and the interference between coherent lasing modes.

The PIN/HBT/VCSEL switch was also used as both a transmitter and a receiver in optical transmission through optical fibers. Using switches that were used in the 500 Mb/s switching experiments, we modulated the switch at a data rate of between 650 Mb/s and 1 Gb/s, and transmitted the optical data through fibers with varying lengths, at the end of which it is detected by another switch and converted into electrical data. Again, single-mode transmssion experienced a BER floor caused by mode-selective loss, but multi-mode transmission was successfully demonstrated at 650 Mb/s across a 1 km span of fiber. The sensitivity of the switch as receiver is somewhat low (-14 dBm at 1 Gb/s) and BER=10^{-9}, and this is an area in which future switch designs must address. Different receiver circuits will be needed to improve the sensitivity of the receiver, and a different photodetector may also be needed to enhanced the responsivity of the detector (~50% quantum efficiency with 30% Fresnel loss). A future switch design will need to incorporate higher eelectronic gain, using multiple gain stages. For the very short distances that exist within a backplane environment, this may not be necessary, and improved component performance will likely suffice.

3. Future Prospects for this Technology:

In this program, we have successfully completed, indeed surpassed goals that we set out to achieve. We have defined and implemented a novel optical switching

architecture, developed the integrated optoelectronics technology needed to implement it, and demonstrated the operation of a multi-stage optical switching network. We have thus fulfilled all of the milestones and more. However, our achievements to date are far from representative of the ultimate performance limit of this technology, which we have only begun to develop.

From the component viewpoint, we have only used 10% of the modulation bandwidth that the VCSEL (10 GHz), the PIN (>10 GHz) or the HBT (>50 GHz) is capable of, and the switching speed that can be achieved can be an order of magnitude higher (~5-10 Gb/s) than we have achieved. Nor have we fully exploited the very low switching energy that is available with a threshold switch with high optical gain. By pre-biasing each switch near threshold, and using switches with a higher differential optical gain (e.g., >20 per stage) switching can be achieved by very-low-energy optical input pulses and still provide sufficient optical gain and energy to be detected by the next switch stage. We have already demonstrated a switching energy in the 300 fJ range, and this can be significantly lowered. The sensitivity of the receiver can also be substantially increased, as we have mentioned above, so that a sensivitiy of <-25 dBm should be achievable at 1 Gb/s. An important criterion in any array performance is the density of power dissipation and thermal self-heating. The power dissipation of each switch stage can be reduced significantly (10x) from its present value (30 mW per switch, operating at 4V and 7.5 mA) to less than <2.5 mW per switch (2.5 V and 1 mA). This can be achieved by using low-threshold, oxide-confined VCSELs with submilliampere operating currents (e.g. 0.3 mA threshold, outputting 200 μW optical power at 1 mA, with a wall-plug efficiency of 20%). This can reduce the operating voltage of the switch to <2 V and its operating current to < 1 mA. A 16x16 array of switches each dissipating 2 mW will have a total dissipation of ~512 mW spread out across a 4 mm x 4 mm area (3 W/cm^2), which is quite manageable.

Perhaps the most promising potential for this technology will be achieved when it is combined with other multiplexing platforms, such as wavelength-division multiplexing (WDM). For example, if each element (or column in a 2D array)) of the switch array is assigned a different lasing wavelength, and selectively detects the same wavelength, then then all of the outputs can be wavelength-multiplexed together onto an optical fiber while keeping the SDM switching architecture intact and projecting it across much larger physical distances. For a 2D array, a linear fiber ribbon array will suffice to project these interconnections over LAN-like distances. The only technology modification needed would be a means of chirping the wavelengths of a VCSEL or photodetector array. A wavelength-selective photodetector array would enjoy the benefit of improved optical crosstalk suppression.

4. Students Supported by this Program:

During its 4 year and 4 months duration, this program has supported, in whole or in part, the efforts of several graduate students. The main contributors to the

research effort were my graduate students Bo Lu, Ping Zhou, and Yin-Chen Lu, who have since completed their Ph.D. degrees and are now gainfully employed in the U.S. optoelectronics or communications industries. It has also in part supported the activities of Geraldo Ortiz, who will soon complete his Ph.D. The program also supported in part the epitaxial material development effort at the UNM Center for High Technology Materials, which grew some of the epitaxial material for this project by MOCVD.

5. Publications:

[1] Bo Lu, Ping Zhou, Y.C.Lu, J. Cheng, R.E. Leibenguth, A. C. Adams, J. L. Zilko, K. L. Lear, J. C. Zolper, S.A. Chalmers, G. A. Vawter, "Monolithic Array of Reconfigurable Binary Optical Switches with Fan-out for Multi-Stage Switching and Interconnection Applications", Integrated Photonics Research Conference, pp. 258-259, Feb. 17-19, 1994.

[2] Bo Lu, Ping Zhou, Y.C.Lu, J. Cheng, R.E. Leibenguth, A. C. Adams, J. L. Zilko, J. C. Zolper, K. L. Lear, S.A. Chalmers, G. A. Vawter, "Reconfigurable Binary Optical Routing Switches with Fan-out Based on the Integration of GaAs/AlGaAs Surface-Emitting Lasers and Heterojunction Phototransistors", IEEE Photonics Technology Letters, Vol. 6, No. 2, pp. 222-226, February 1994.

[3] Bo Lu, Ping Zhou, Y.C.Lu, J. Cheng, R.E. Leibenguth, A. C. Adams, J. L. Zilko, K. L. Lear, J. C. Zolper, S.A. Chalmers, G. A. Vawter, "Binary Optical Switch and Programmable Optical Logic Gate Based on the Integration of GaAs/AlGaAs Surface-Emitting Lasers and Heterojunction Phototransistors", IEEE Photonics Technology Letters, Vol.6, No. 3, pp. 398-401, March 1994.

[4] Ping Zhou, Bo Lu, J. Cheng, K. J. Malloy, "Efficient Vertical-Cavity Surface-Emitting Lasers with a Thermally Stable Threshold Voltage and a Wide cw Operating Temperature Range (90K to 400K)", Technical Digest of the 1994 Conference on Lasers and Electro-Optics 1994, Vol. 8, pp.29-30, 1994, Paper CMI3.

[5] Bo Lu, Ping Zhou, Yin-Chen Lu, Julian Cheng, R. E. Leibenguth, A. C. Adams, J. L. Zilko, J. C. Zolper, K. L. Lear, S. A. Chalmers, and G. A. Vawter, "Reconfigurable Optical Logic Gate and Routing Switch Based on the Monolithic Integration of Surface-Emitting Lasers and Heterojunction Phototransistors", Technical Digest of the 1994 Conference on Lasers and Electro-Optics 1994, Vol. 8, pp.375-376, 1994, Paper CThP3.

[6] Bo Lu, Ping Zhou, Julian Cheng, K.J.Malloy, "Simulation of the temperature dependence of Vertical-Cavity Surface-Emitting Laser Threshold Current", OELASE 1994, Vol. 2147 on Vertical Cavity Surface Emitting Laser Arrays, pp. 12-21, 1994.

[7] G. G. Ortiz, Julian Cheng, "High-speed Modulation and Small-signal Circuit Modeling of Deeply-Implanted VCSELs with a GRINSCH Active Layer and Graded

Heterointerfaces", SPIE Vol. 2147, Vertical Cavity Surface Emitting Laser Arrays, pp. 28-39,1994.

[8] J. Cheng, P. Zhou, J. C. Zolper, K. L. Lear, G. A. Vawter, R. E. Leibenguth, A.C. Adams, "Reconfigurable Optical Switches with Monolithic Electrical-to-Optical Interfaces", SPIE Vol. 2153, Optoelectronic Interconnects II, pp. 315-322,1994.

[9] J. Cheng, P. Zhou, B. Lu, R.E.Leibenguth, A. C. Adams, J. A. Zopler, G. A. Vawter, S. A. Chalmers,"Monolithic photonic and optoelectronic technology for high-speed switching networks, reconfigurable optical interconnects, and optical data processing, SPIE Vol. 2155, Optoelectronic Signal Processing for Phased-Array Antennas IV, 1994.

[10] J. Cheng, B. Lu, J. C. Zolper, K.L. Lear, J. Klemm, "Monolithic Binary Optical Logic Gates with Programmable Optical Routing", LEOS 1994 Summer Topical Meeting Digest on Integrated Optoelectronics, pp. 19-20, July 6-8, 1994.

[11] Bo Lu, P. Zhou, J. Cheng, K. J. Malloy, "High Temperature Pulsed and CW Operation and Thermally Stable Threshold Characteristics of Vertical-Cavity Surface-Emitting Lasers Grown by MOCVD", Appl. Phys. Lett., Vol. 65, No. 11, pp. 1337-1339,1994.

[12] Julian Cheng, "Monolithic Optical Switching Technology for a Programmable Optical Logic Gate Array", Optics and Laser Technology, Special Issue on Optical Computing, Vol. 26, No. 4, pp.239-249, 1994.

[13] P. Zhou, B. Lu, J. Cheng, K. Malloy, J. C. Zolper, "Vertical-Cavity Surface-Emitting Lasers with Thermally Stable Electrical Characteristics", J. Appl. Phys., March 1995.

[14] Y. C. Lu, J. Cheng, P. Zhou, J. Klem, J. C. Zolper, "High Speed Electrical and Optical Modulation Response of Monolithic Switches Integrating a Heterojunction Phototransistor with a Surface-Emitting Laser", Electronics Lett., March 1995.

[15] (Invited) Julian Cheng, Y.-C. Lu, B. Lu, J. C. Zolper, J. Klem, K. L. Lear, "The Monolithic Integration of Vertical-Cavity Surface-Emitting Lasers with Optical and Electronic Devices for High Speed Optical Interconnects", Proc. of 1995 SPIE Conference on Optical Interconnects III.

TECHNICAL TALKS:

[1] Bo Lu, Ping Zhou, Y.C.Lu, J. Cheng, R.E. Leibenguth, A. C. Adams, J. L. Zilko, K. L. Lear, J. C. Zolper, S.A. Chalmers, G. A. Vawter, "Monolithic Array of Reconfigurable Binary Optical Switches with Fan-out for Multi-Stage Switching and Interconnection Applications", 1994 Technical Digest of the Integrated Photonics Research Conference, pp. 259-259, Feb. 1994.

[2] J. Cheng (Invited), "Reconfigurable Optical Switches and Optical Routing Networks", 1994 Workshop on Compound Semiconductor Materials and Devices (WOCSEMMAD), San Francisco, CA; Feb. 21-23, 1994.

[3] Julian Cheng, Bo Lu, Ping Zhou, K.J.Malloy, "Simulation of the temperature dependence of Vertical-Cavity Surface-Emitting Laser Threshold Current", OELASE 1994, VCSEL Arrays, Los Angeles, CA, Jan. 26, 1994.

[4] Bo Lu, Ping Zhou, Julian Cheng, K.J.Malloy, "Optimized Design of Vertical-Cavity Surface-Emitting Lasers", OELASE 1994, Physics and Simulation of Optoelectronic Devices II, Los Angeles, CA; Jan. 27, 1994.

[5] G. G. Ortiz, Julian Cheng, "High-speed Modulation and Small-signal Circuit Modeling of Deeply-Implanted VCSELs with a GRINSCH Active Layer and Graded Heterointerfaces", OELASE 1994, VCSEL Arrays, Los Angeles, CA; Jan. 27, 1994.

[6] J. Cheng, "Reconfigurable Optical switches with Monolithic Electrical-to-Optical Interfaces", OELASE Optoelectronic Interconnects II, Los Angeles, CA, Jan. 27, 1994.

[7] J. Cheng, B. Lu, R.E.Leibenguth, A. C. Adams, J. A. Zopler, G. A. Vawter, S. A. Chalmers,"Monolithic photonic and optoelectronic technology for high-speed switching networks, reconfigurable optical interconnects, and optical data processing, OELASE 1994, Optoelectronic Signal Processing for Phased-Array Antennas IV, Los Angeles, CA, Jan. 27, 1994.

[8] Ping Zhou, Bo Lu, J. Cheng, K. J. Malloy, "Efficient Vertical-Cavity Surface-Emitting Lasers with a Thermally Stable Threshold Voltage and a Wide cw Operating Temperature Range (90K to 400K)", CLEO 1994, paper CMI3.

[9] Bo Lu, Ping Zhou, Yin-Chen Lu, Julian Cheng, R. E. Leibenguth, A. C. Adams, J. L. Zilko, J. C. Zolper, K. L. Lear, S. A. Chalmers, and G. A. Vawter, "Reconfigurable Optical Logic Gate and Routing Switch Based on the Monolithic Integration of Surface-Emitting Lasers and Heterojunction Phototransistors", CLEO 1994, Paper CThP3.

[10] J. Cheng, B. Lu, J. C. Zolper, K.L. Lear, J. Klemm, "Monolithic Binary Optical Logic Gates with Programmable Optical Routing", LEOS 1994 Summer Topical Meeting Digest on Integrated Optoelectronics; July 8, 1994.

[11] Julian Cheng, "Optoelectronic Multi-Processor Interconnects", Engineering Foundation Workshop on High Speed Optical Interconnects, August 14-18, San Luis Obispo, CA.

6. Figure Captions:

Figure 1. (a) The photomicrograph, (b) device structure, and (c) electrical and lasing characteristics of a proton-implant-isolated VCSEL (above) and an oxide-confined VCSEL (below).

Figure 2. (a) The proton-implant-isolated structure, (b) electrical characteristics, and (c) lasing characteristics of a typical 16 μm diameter VCSEL with continuous, bi-parabolically-graded DBR mirror heterointerfaces grown by MOCVD. Low operating voltages and high power conversion efficiency are achieved.

Figure 3. The optical transmission characteristics of a VCSEL based optical link using (a) different lengths of a single mode optical fiber at 650 Mb/s, and (b) a 1 km length of graded-index multi-mode fiber at 1 Gb/s.

Figure 4. A generic parallel optical array processor using 2D arrays of VCSELs and other VCSEL-based switches, detectors, and logic gates, which can perform a variety of different functions, including switching, logic, routing, and memory.

Figure 5. A reconfigurable, closed-ring, optical interconnect architecture linking clusters of nodes through parallel optical paths set by optoelectronic switch arrays, which contain electrical input and output ports. Each switch contains a segmented HPT interconnected individually to different VCSELs in the array, and can be programmed to receive, transmit, or re-route optical signals. Schematic layout of a two-stage optical backplane interconnecting 4 electronic processors (2 per stage). Each processor contains an optoelectronic interface to the switch, through which it can transmit or receive optical data, as well as to bypass the incoming optical data or to re-route it to another stage.

Figure 6. A reconfigurable, board-to-board, multi-stage optical interconnection network. Each board contains a number of processors with parallel access to a parallel optical data bus, whose traffic is regulated by a two-dimensional array of optical switches on each board, each of which can communicate directly with an electronic processor on that board.

Figure 7. Three different classses of optical switches based on the monolithic integration of a VCSEL with (a) a heterojunction phototransistor (HPT), (c) a photothyristor (PNPN), and (b) a photothyristor with modified positive feedback.

Figure 8. The optical switching characteristics (above) and electrical characteristics (below) of the three types of optical switches that are described in figure 7, which have (a) non-latching, (b) bistable, and (c) latching characteristics, respectively.

Figure 9. The epilayer structure, photomicrograph, and circuit design of monolithic, (a) 2x2 and (b) 1x2, binary optical routing switches with optical fan-out. The 2x2 switch is a combination of two 1x2 switches. Also shown schematically

are the modes of operation for each switch, including routing, fan-out, bypass and exchange.

Fig. 10. (a) The routing functions and photomicrograph of a reconfigurable 1x2 binary HPT/VCSEL optical switch, which can be dynamically reconfigured to route input optical data to different optical output ports with fan-out. (b) Experimental demonstration of 1x2 optical switching, showing the routing control voltages and the optical output channels for the cases of (a) no fan-out, and (b) an optical fan-out of 2.

Fig. 11. (a) The routing functions and photomicrograph of a reconfigurable 2x2 binary HPT/VCSEL optical switch, which can be dynamically reconfigured to perform optical bypass and exchange routing operations. (b) Experimental demonstration of 2x2 optical switching, showing the control voltages, the input and output optical channels, and the bypass and exchange operations.

Fig. 12. A linear array of reconfigurable binary HPT/VCSEL switches, which can be programmed to perform different optical logic and spatial routing functions with variable optical fan-out by setting the control voltages of each switch (as shown). Each node contains a two-segment HPT, whose segments are connected to different VCSELs in a shuffle network geometry. Different arrays of switches with the same routing geometry can be optically cascaded to perform more complex functions.

Figure 13. (Below) The epilayer design and device layout of a monolithic optoelectronic switch integrating a VCSEL with a HBT, which provides a rudimentary optoelectronic interface between the optical switching fabric and an electronic processor, which modulates the VCSEL to produce an optical output. Also shown (above) are the electrical and optical characteristics of the switch and its electrical-to-optical conversion efficiency.

Figure 14. (a) The experimental setup for measuring the high-frequency modulation response of a monolithic three-terminal HPT/VCSEL switch, (b) shows the small-signal response of the HPT and the switch, and (c) shows its large-signal modulation characteristics at 500 Mb/s.

Figure 15. (a) A monolithic HBT/VCSEL switch using an improved self-aligned HBT, (b) its common-emitter characteristics, (c) its current gain, and (d) its modulatiuon response.

Figure 16. (a) Photomicrograph, and (b) epilayer structure of a monolithic HPT/VCSEL switch. (c) Schematic diagram of the emitter-follow circuit, with optical input P_{in}, electrical input E_{in}, optical output P_{out}, and electrical output I_{out}, (d) Time traces showing the electrical (trace 3) and optical (trace 4) output of the switch in response to the combined electrical (trace 1) and optical (trace 2) input data at 200 Mb/s. Each output contains replicas of both inputs. (e) Eye-diagrams showing the optical (lower traces) and electrical (upper traces) response of the switch to large-signal, pseudorandom modulation by optical (left) and electrical (right) input data at 200 Mb/s.

Figure 17. (a) The circuit design, (b) epilayer structure, and (c) photomicrograph of a binary PIN/HBT/VCSEL routing switch containing a segmented PIN input port and two VCSEL output ports. The lower traces show the optical output of the switch in response to (d) electrical, and (e) optical input modulation at a data rate of 400 Mb/s, while (f) shows the optical output from VCSEL A and VCSEL B of the binary optical switch in response to optical input modulation at 500 Mb/s, showing that the switched output emerges alternately from output channel A or output channel B as the routing control voltage is toggled between the two individual switches.

Figure 18. Epilayer structure and circuit layout of a modified binary HBT/PIN/VCSEL switch, which uses a common p-substrate configuration for the VCSEL to achieve a switching circuit design with improved speed performance.

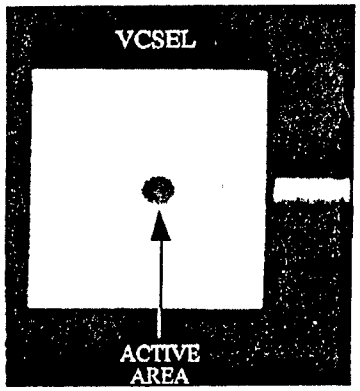
Figure 19. Optically-cascaded, multi-stage switching and routing operation using three arrays of binary PIN/HBT/VCSEL switches, which provide multi-point optical interconnections between different input and output nodes. The photomicrograph shows the experimental array.

Figure 20. The experimental setup used to demonstrate optically-cascaded, multi-stage switching operation.

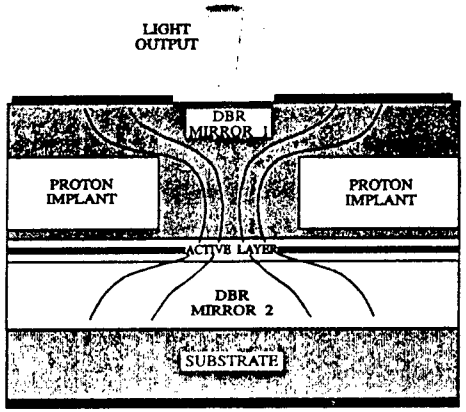
Figure 21. (a) The circuit design, and (b) layout of a reconfigurable binary PIN/HBT/VCSEL optical routing switch. (c) shows an optically-cascaded, multi-stage switching network using arrays of binary switches to perform the optical routing functions. (d) shows the common-emitter characteristics of the HBT, (e) shows the electrical and lasing characteristics of the VCSEL, and (f) shows the differential optical gain of each each of the two stages under optically cascaded dc switching operation.

DESIGN AND CHARACTERISTICS OF VERTICAL-CAVITY SURFACE-EMITTING LASER STRUCTURES

Julian Cheng, University of New Mexico, Center for High Technology Materials

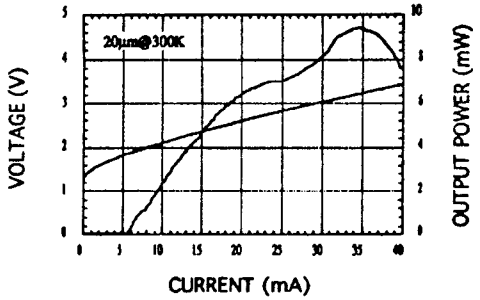


Proton-Implant-Isolated VCSEL

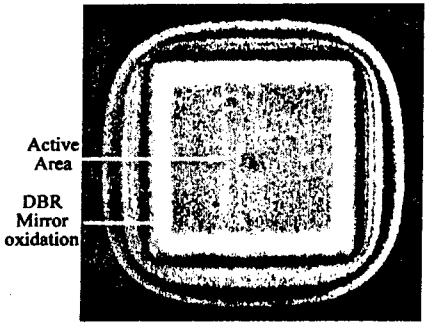


Characteristics of Proton-Implant-Isolated VCSEL

20 μ m DIAMETER, 300K, PARABOLIC GRADING

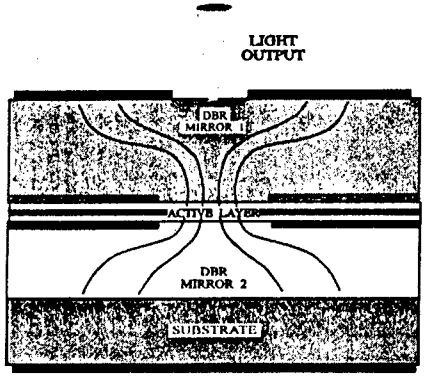


Oxide-Confined VCSEL



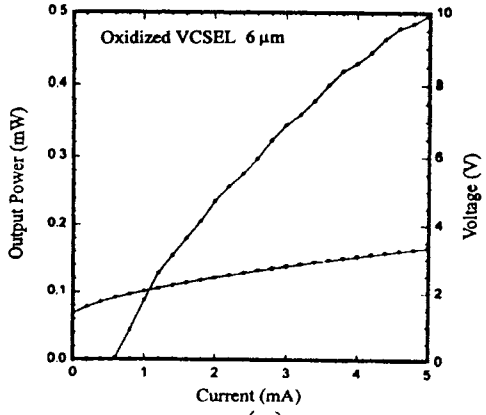
(a)

Planar, Low-Threshold Oxide-Confined VCSEL



(b)

Characteristics of Oxide-Confined VCSEL at 300K



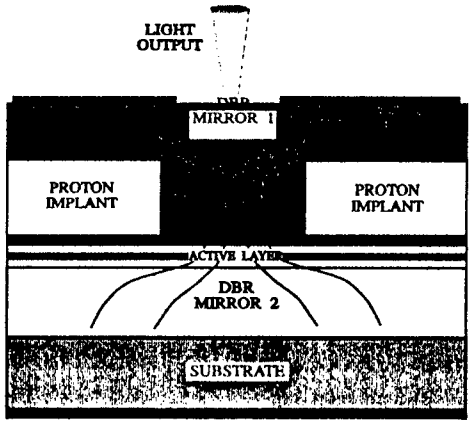
(c)

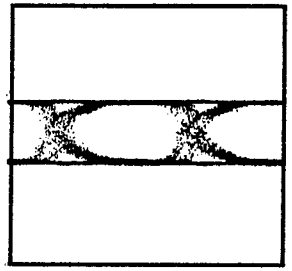
Fig 1

UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS
JULIAN CHENG

HIGH PERFORMANCE VCSELS FOR OPTICAL INTERCONNECTS

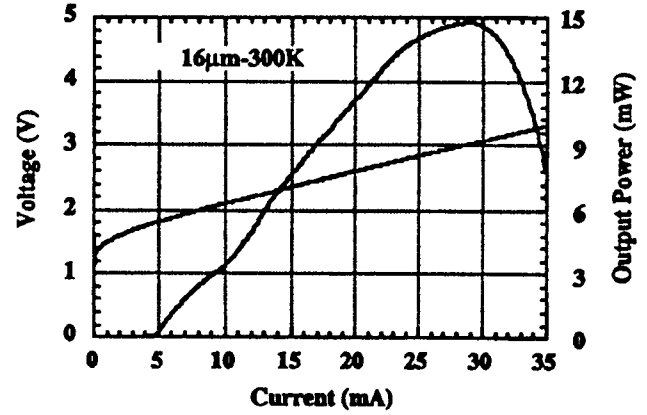
PROTON-IMPLANT-ISOLATED VCSEL





200 ps/div.

1 Gb/s, (2^{23}-1) NRZ, PRBS Data Transmission through 1km of Multi-Mode Fiber
Bit Error Rate < 1E-13



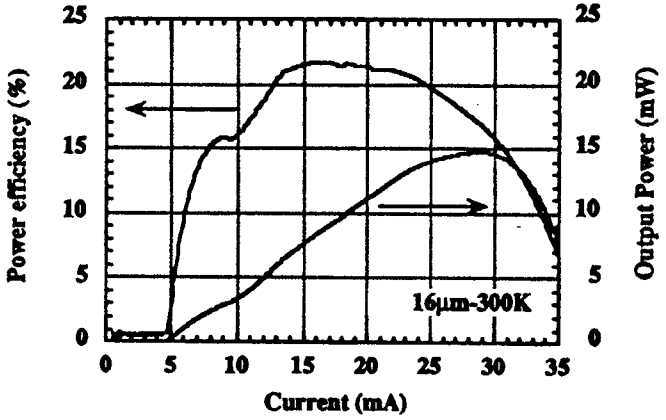
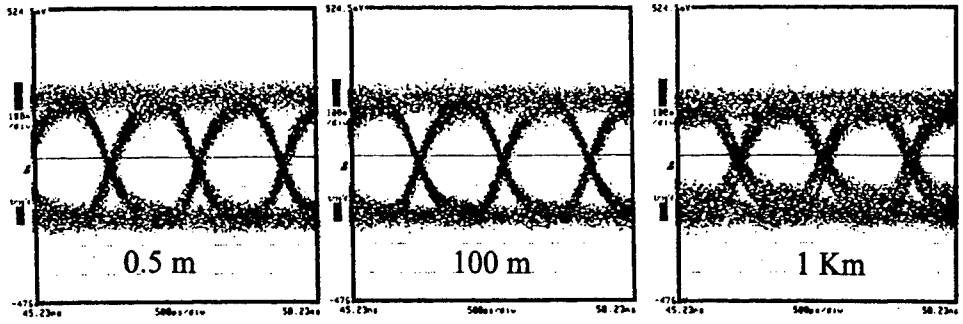


Fig 2

Fig 3

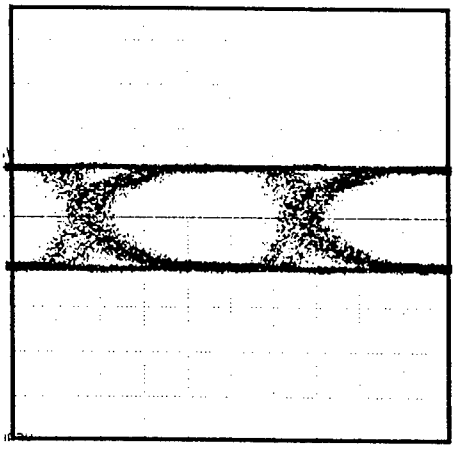
JULIAN CHENG
UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS

650 MB/S TRANSMISSION OF 850 NM VCSEL THROUGH A SINGLE-MODE FIBER



(a)

1 Gb/s, (2^{23}-1) NRZ, PRBS Data Transmission through 1km of Multi-Mode Fiber

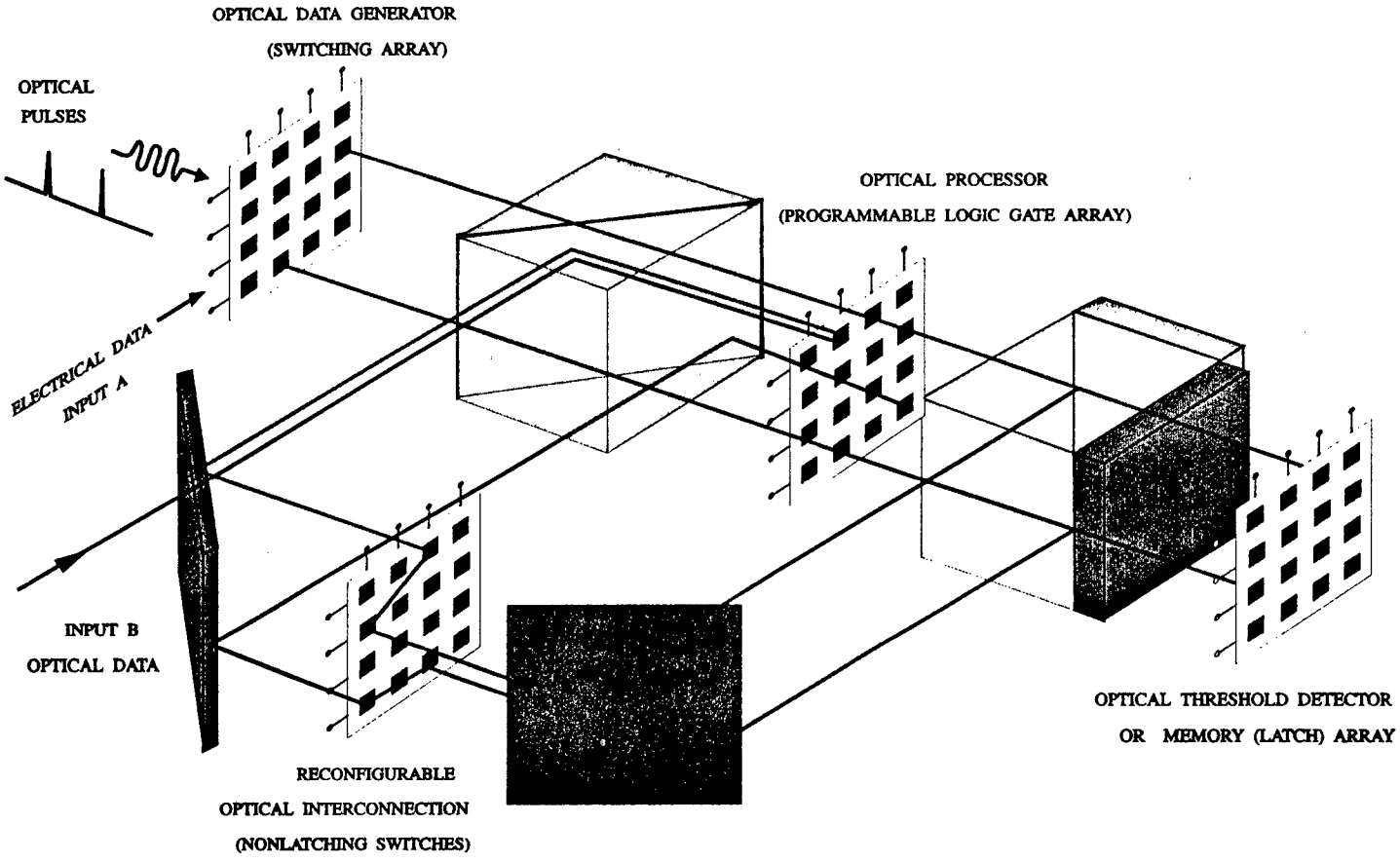


200 ps/div.

Bit Error Rate < 1E-13

(b)

CENTER FOR HIGH TECHNOLOGY MATERIALS
UNIVERSITY OF NEW MEXICO
JULIAN CHENG



PARALLEL OPTICAL ARRAY PROCESSOR

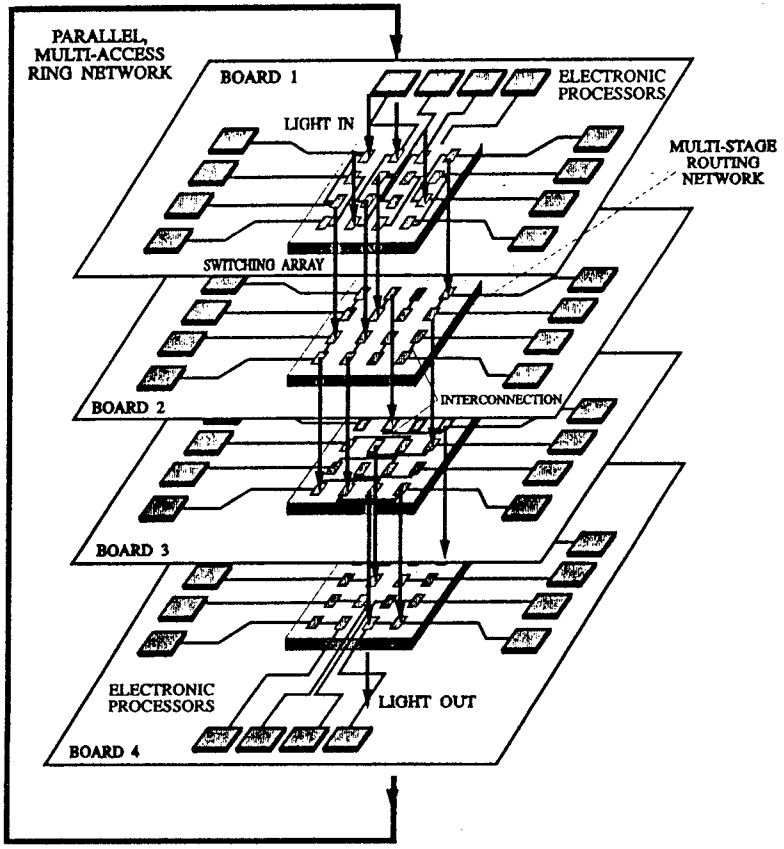
INTEGRATED VCSEL/PHOTOTHYRISTOR AND VCSEL/PHOTOTRANSISTOR OPTICAL SWITCHES

Fig 4

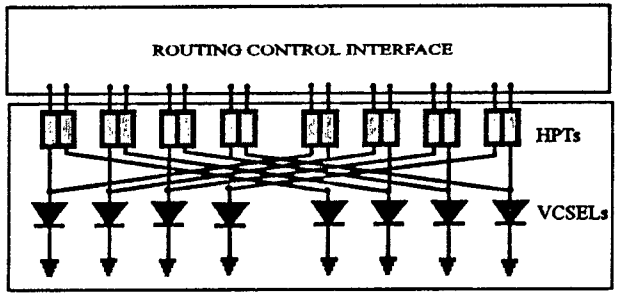
CENTER FOR HIGH TECHNOLOGY MATERIALS
UNIVERSITY OF NEW MEXICO

JULIAN CHENG

TWO-DIMENSIONAL, RECONFIGURABLE INTER-BOARD OPTICAL INTERCONNECT



MONOLITHIC OPTOELECTRONIC SWITCHING FABRIC



INTERPROCESSOR OPTICAL INTERCONNECT

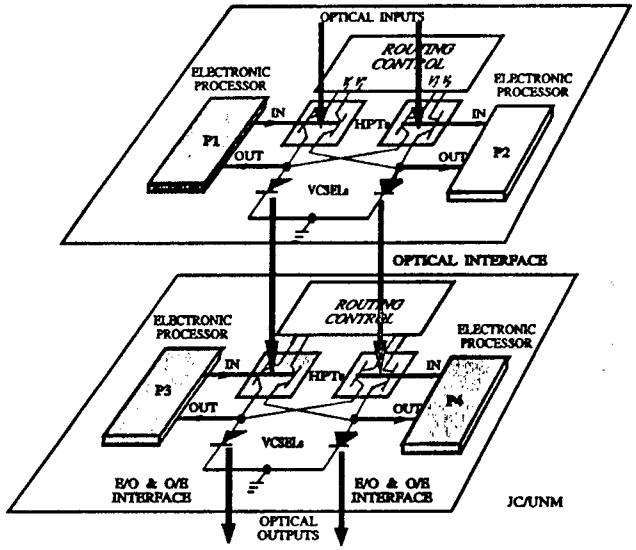
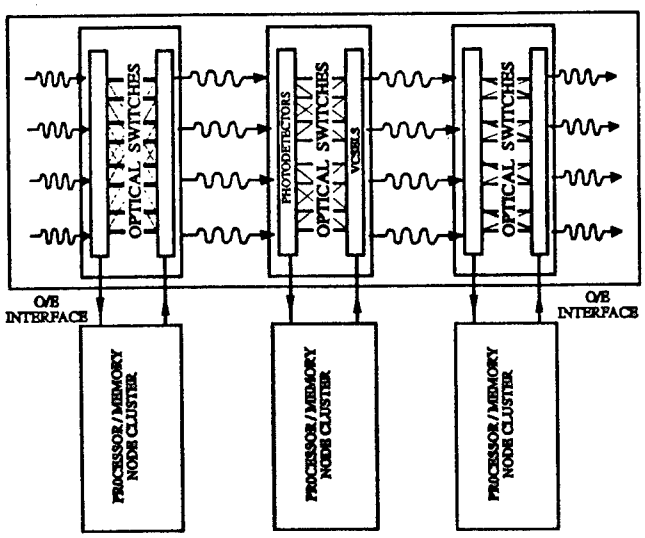


Fig 5

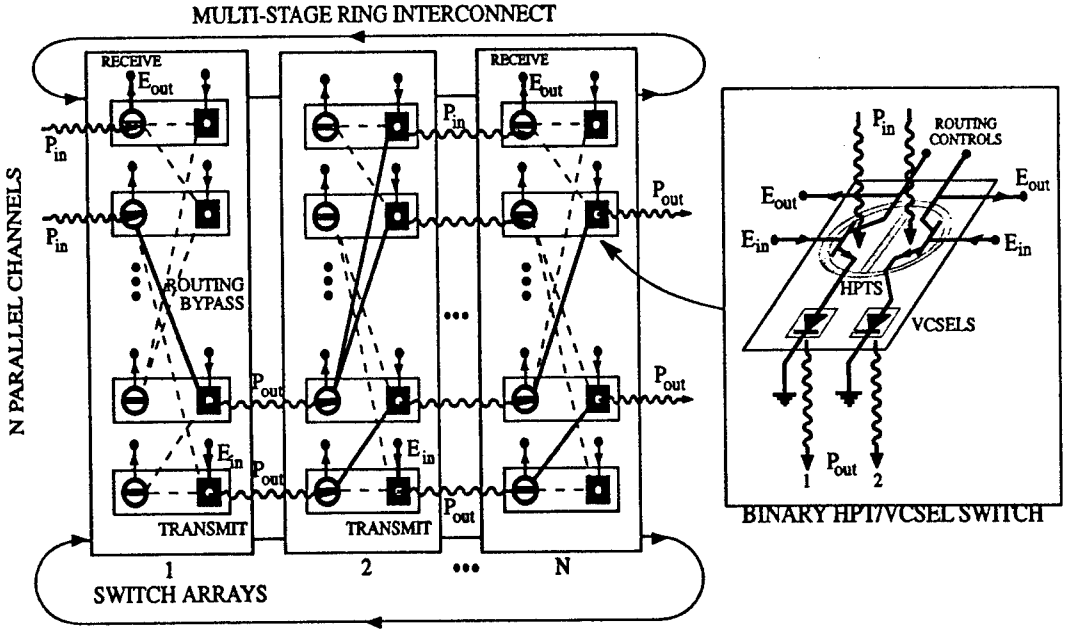
Fig 6

UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS
JULIAN CHENG

RECONFIGURABLE OPTOELECTRONIC SWITCHES AND PARALLEL OPTICAL INTERCONNECT



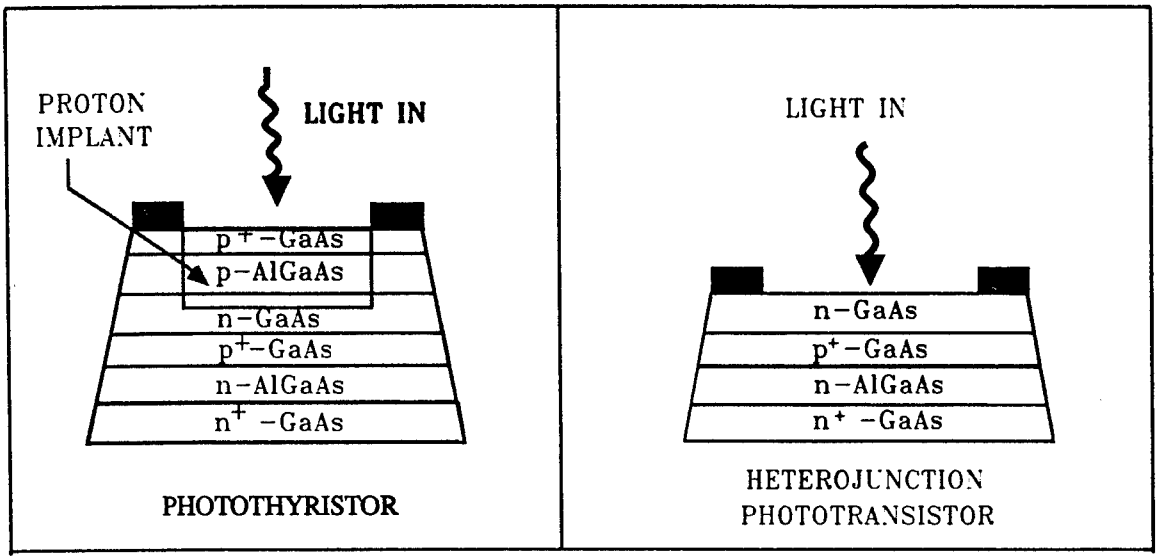
PARALLEL RECONFIGURABLE OPTICAL INTERCONNECT WITH MONOLITHIC OPTOELECTRONIC TRANSCEIVER INTERFACES



JULIAN CHENG
UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS

(B) OPTICALLY BISTABLE SWITCH

(A) NON-LATCHING SWITCH



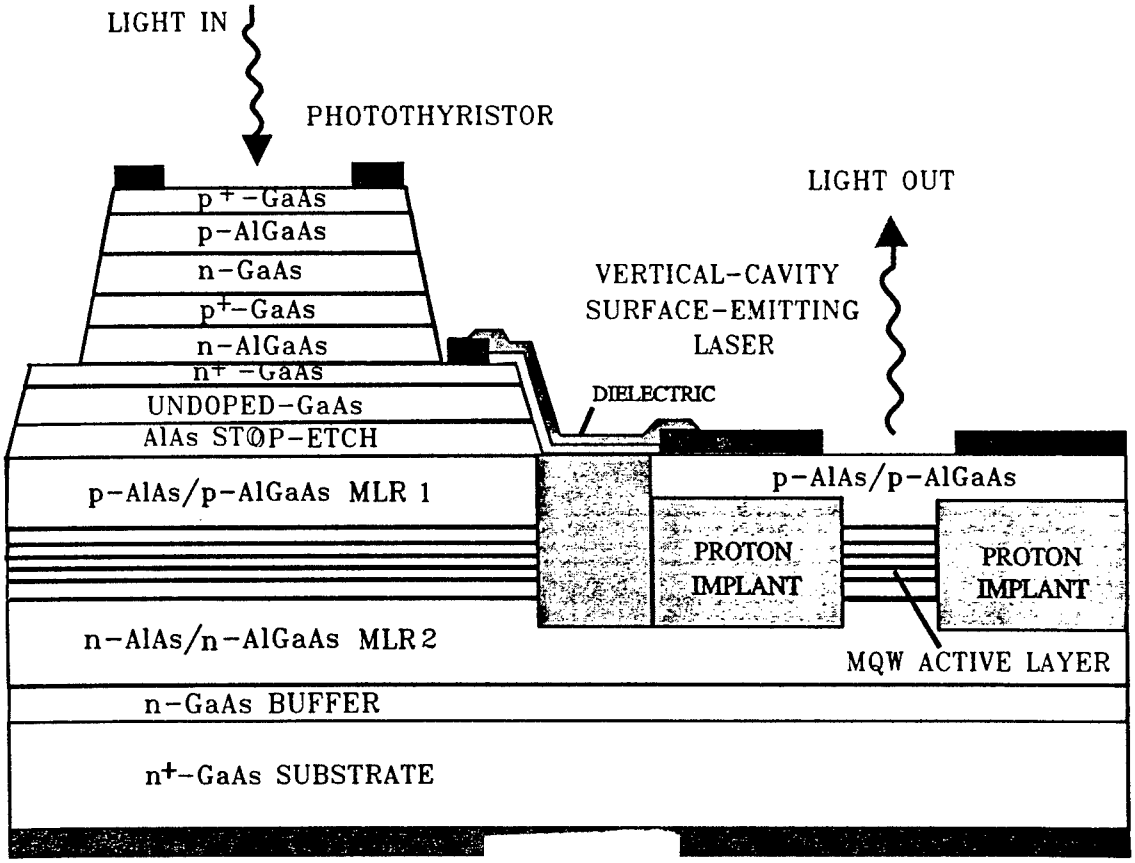
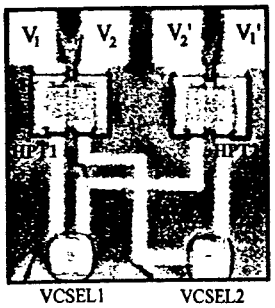


Fig 7

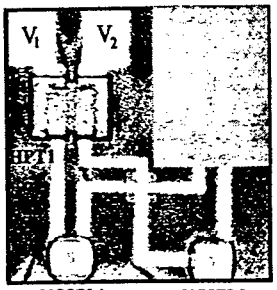
(C) LATCHING OPTICAL SWITCH

UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS
JULIAN CHENG

BINARY SWITCH LAYOUT

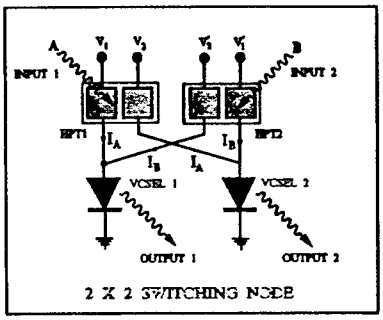


VCSEL1 VCSEL2

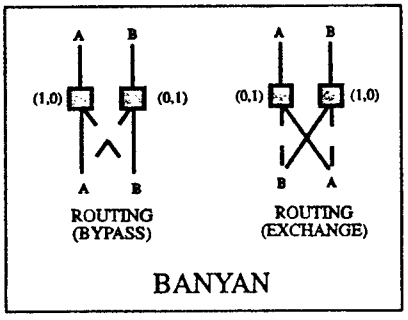


VCSEL1 VCSEL2

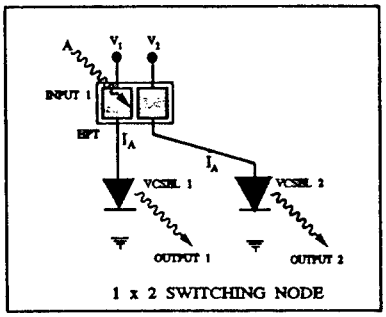
RECONFIGURABLE HPT/VCSEL OPTICAL SWITCHES



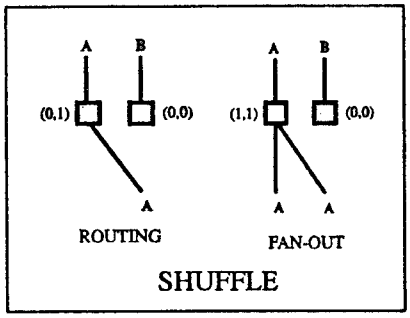
2 X 2 SWITCHING NODE



BANYAN



1 x 2 SWITCHING NODE



SHUFFLE

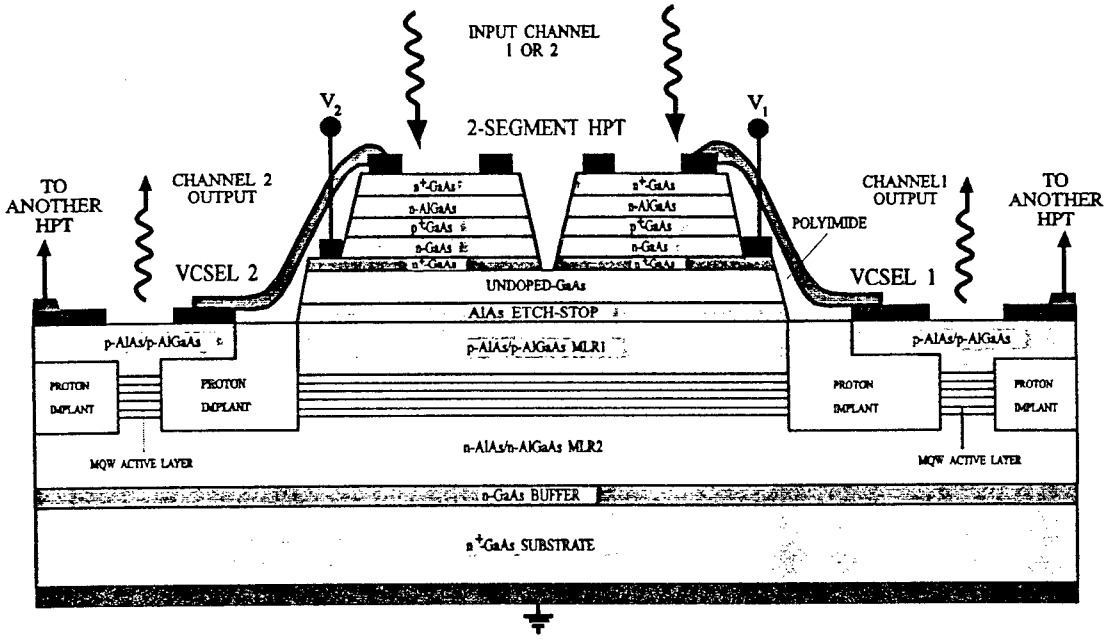
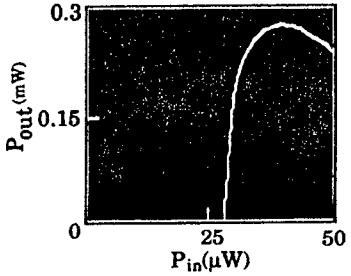


Fig 8

JULIAN CHENG

CENTER FOR HIGH TECHNOLOGY MATERIALS
UNIVERSITY OF NEW MEXICO

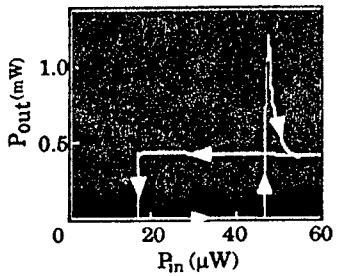
MULTI-FUNCTIONAL PHOTONIC SWITCHES



NON-LATCHING

VCSEL/PHOTOTRANSISTOR SWITCH

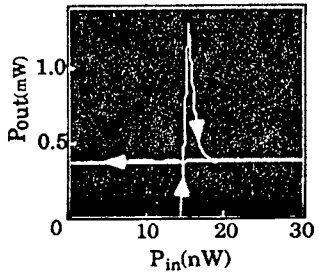
NO POSITIVE FEEDBACK



BISTABLE

VCSEL/PHOTOTHYRISTOR SWITCH

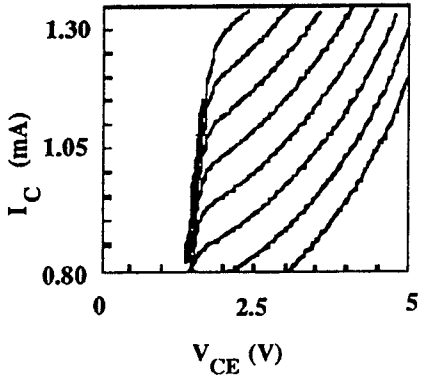
WEAK POSITIVE FEEDBACK

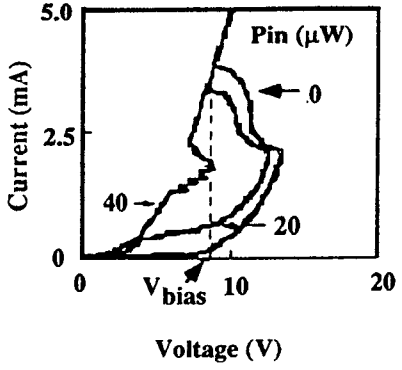


LATCHING

VCSEL/PHOTOTHYRISTOR SWITCH

STRONG POSITIVE FEEDBACK





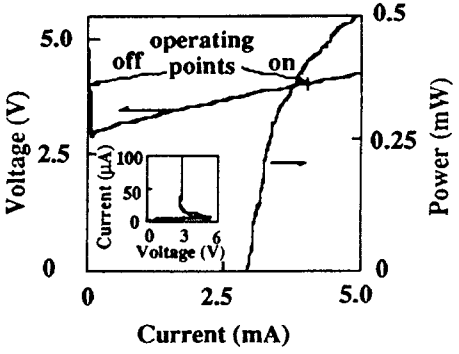


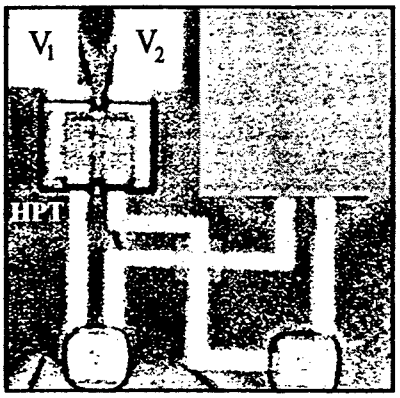
Fig 9

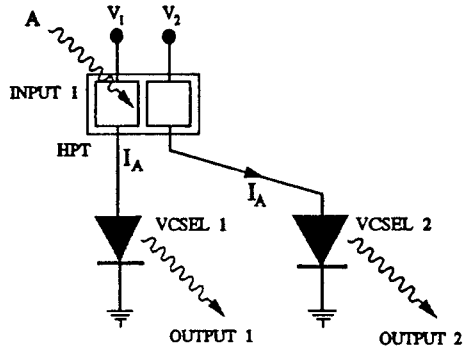
Fig 10

UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS
JULIAN CHENG

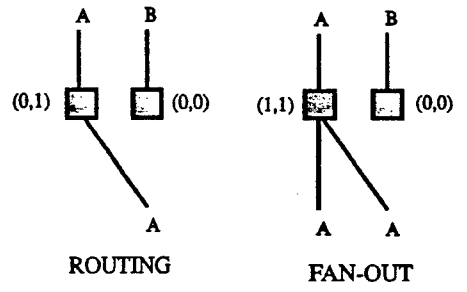
RECONFIGURABLE, MONOLITHIC HPT/VCSEL BINARY OPTICAL ROUTING SWITCH WITH FAN-OUT

1x2 BINARY ROUTING SWITCH

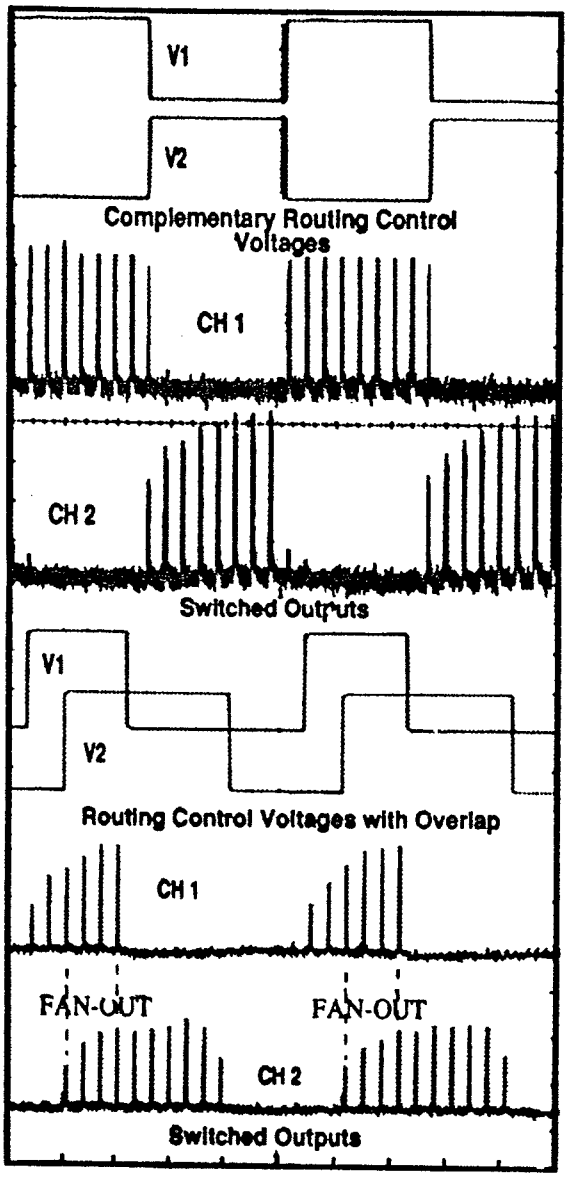




1 x 2 SWITCHING NODE



OPTICAL ROUTING AND FAN-OUT



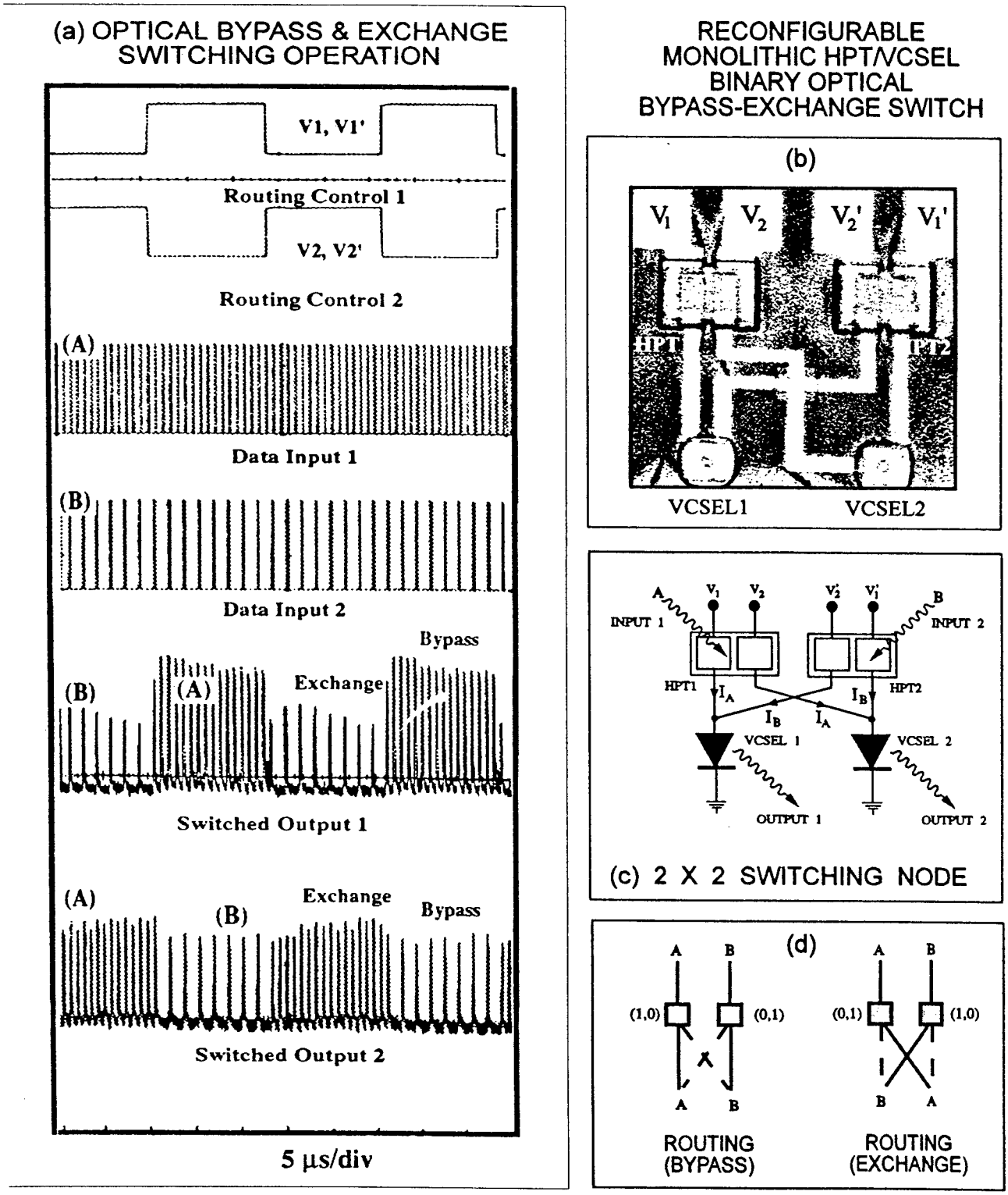
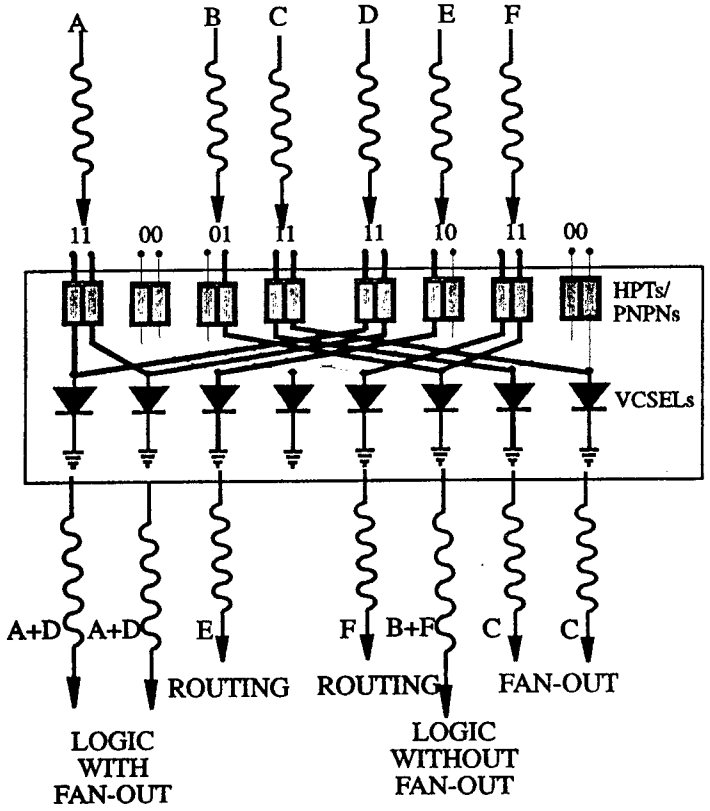


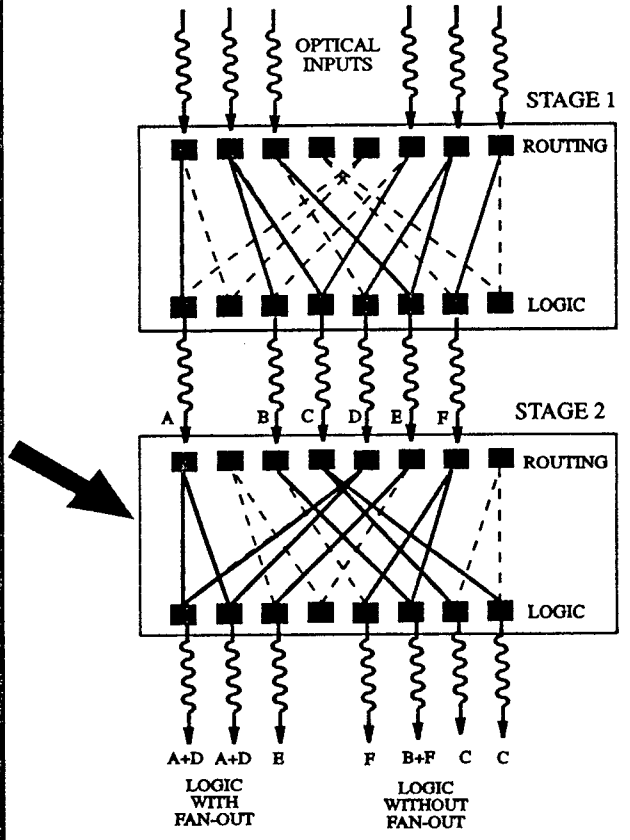
Figure 11 (a) Optical bypass-exchange routing operation using a reconfigurable binary optical routing switch consisting of two pairs of monolithic HPT/VCSEL switches. The switch layout is shown in (b), its circuit diagram in (c), and its switching functions in (d).

JULIAN CHENG
UNIVERSITY OF NEW MEXICO, CENTER FOR HIGH TECHNOLOGY MATERIALS

PROGRAMMABLE OPTICAL SWITCH ARRAY FUNCTIONS



PHYSICAL
IMPLEMENTATION OF
PROGRAMMABLE FUNCTIONS

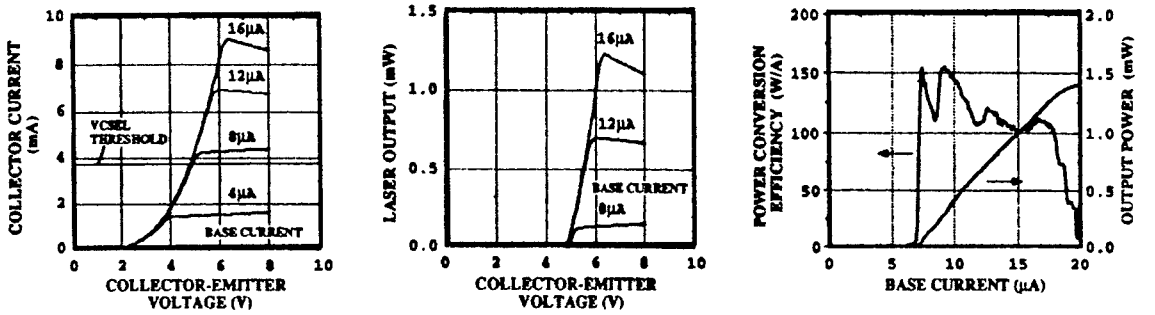


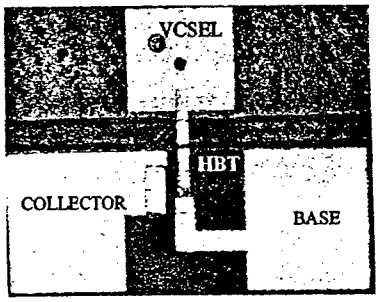
FUNCTIONAL SCHEMATIC OF
PROGRAMMABLE SWITCH ARRAYS

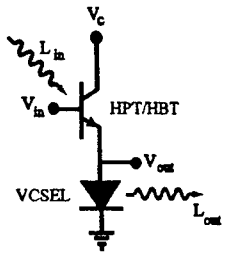
Fig 12

CENTER FOR HIGH TECHNOLOGY MATERIALS
UNIVERSITY OF NEW MEXICO
JULIAN CHENG

MONOLITHIC INTEGRATION OF VERTICAL-CAVITY SURFACE-EMITTING LASERS AND HETEROJUNCTION BIPOLAR TRANSISTORS







HETEROJUNCTION
BIPOLAR TRANSISTOR

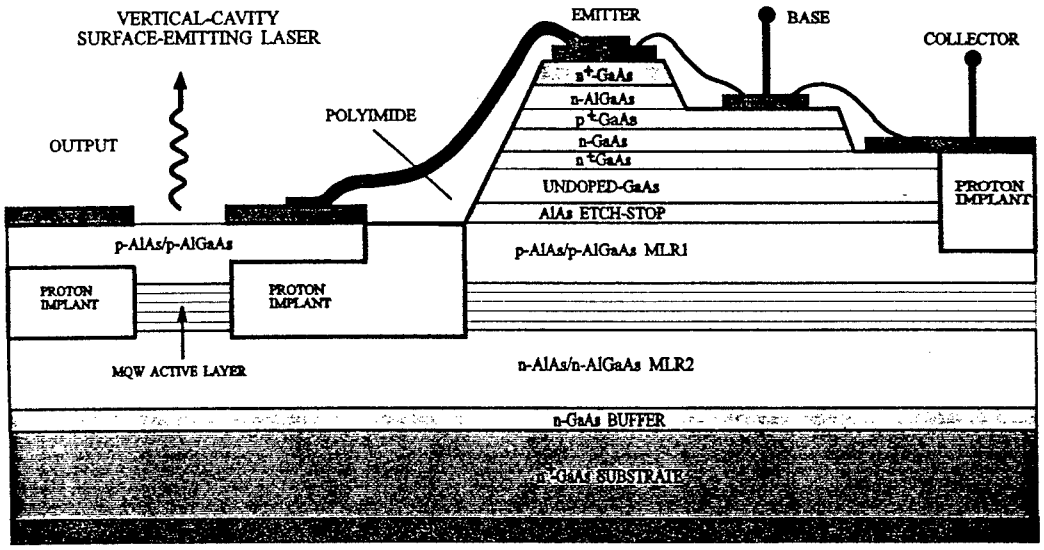
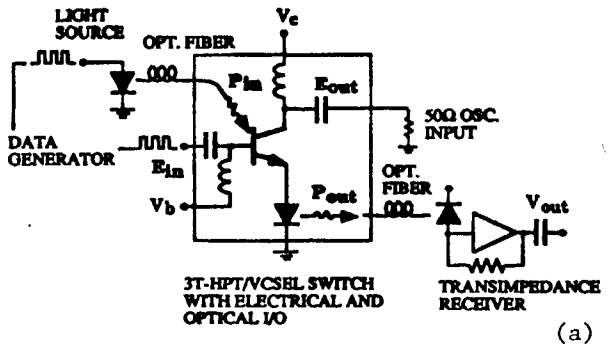


Fig 13

JULIAN CHENG
UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS

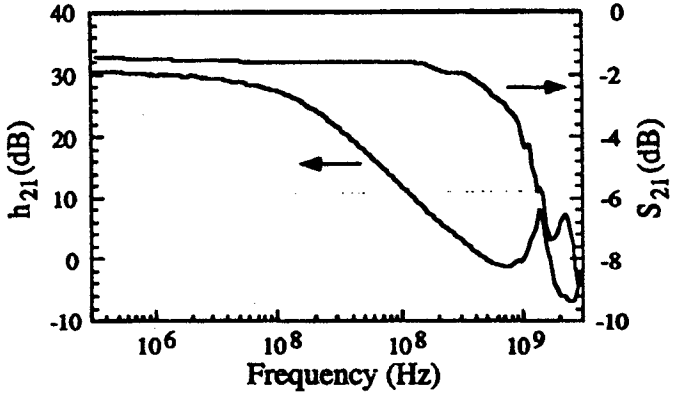
500 Mb/s ELECTRICAL TO OPTICAL MODULATION RESPONSE OF A MONOLITHIC HPT/VCSEL SWITCH

SWITCHING EXPERIMENTAL SET-UP

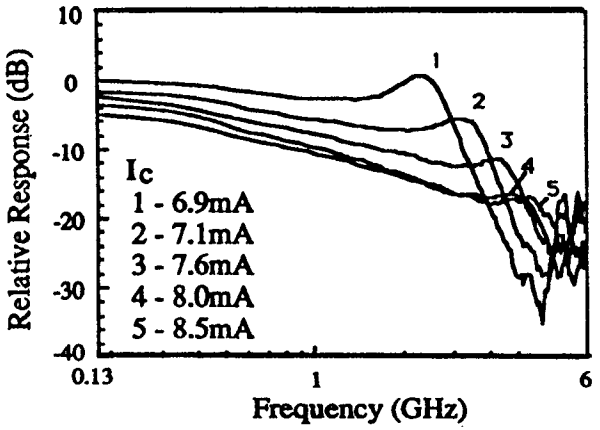


(a)

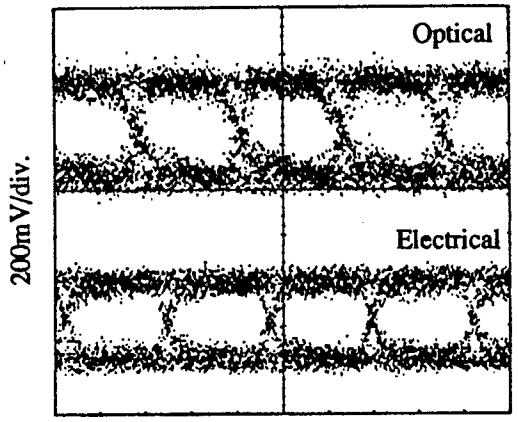
SMALL-SIGNAL MODULATION RESPONSE OF HPT



SMALL-SIGNAL MODULATION RESPONSE OF SWITCH



(b)



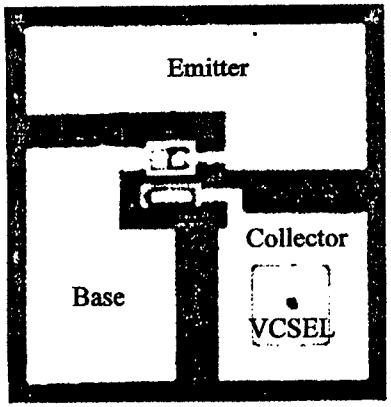
500 Mb/s Eye Diagram

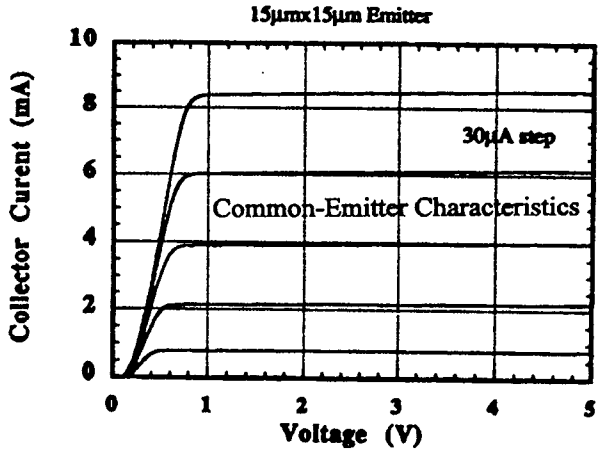
(c)

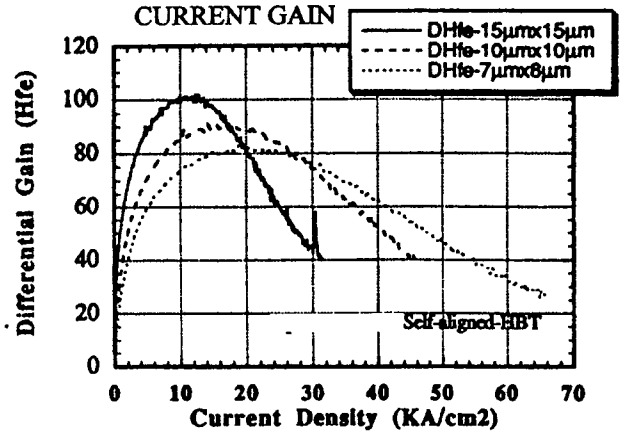
Fig 14

UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS
JULIAN CHENG

HETEROJUNCTION BIPOLAR TRANSISTOR CHARACTERISTICS IN A MONOLITHIC HBT/VCSEL SWITCH







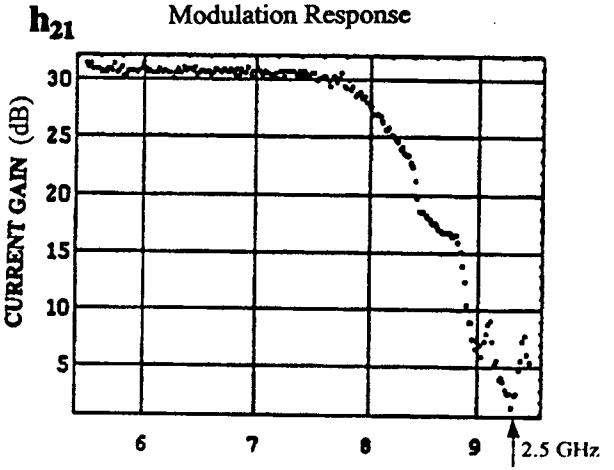
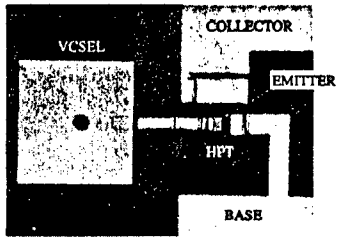


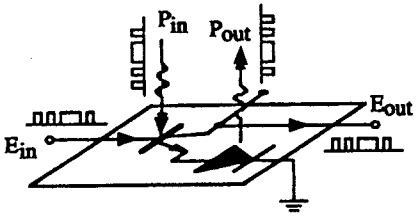
Fig 15

JULIAN CHENG
CENTER FOR HIGH TECHNOLOGY MATERIALS
UNIVERSITY OF NEW MEXICO

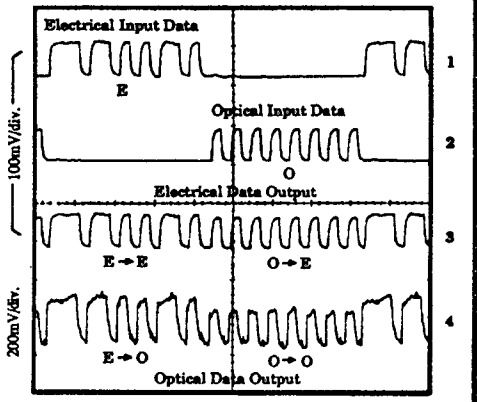
200 Mb/s MODULATION RESPONSE OF A MONOLITHIC HPT/VCSEL OPTICAL SWITCH



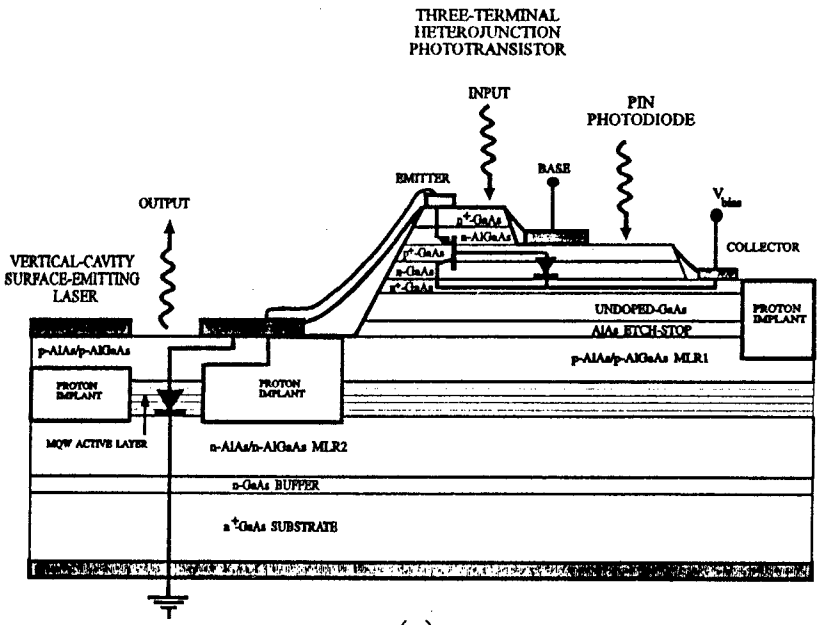
(a)



(b)

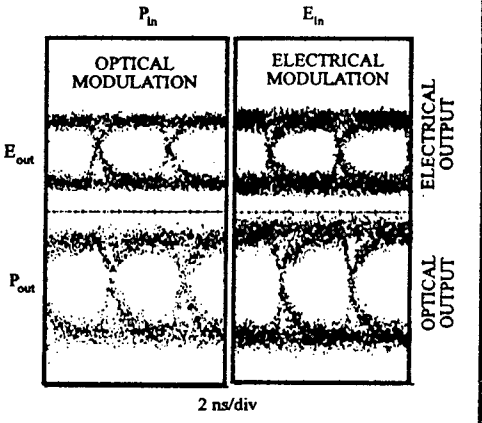


(d)



(c)

(e)

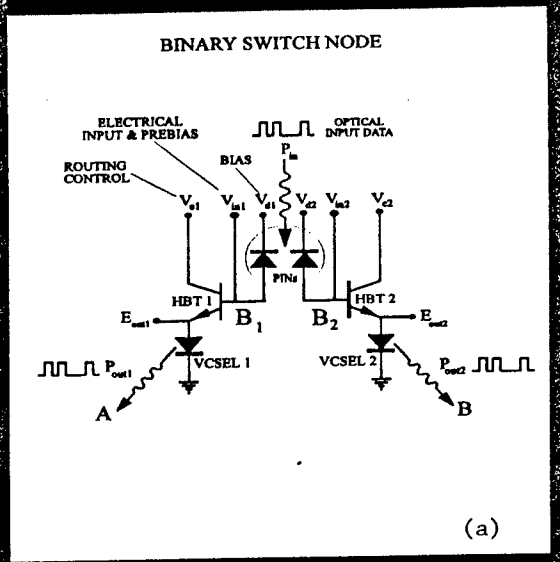


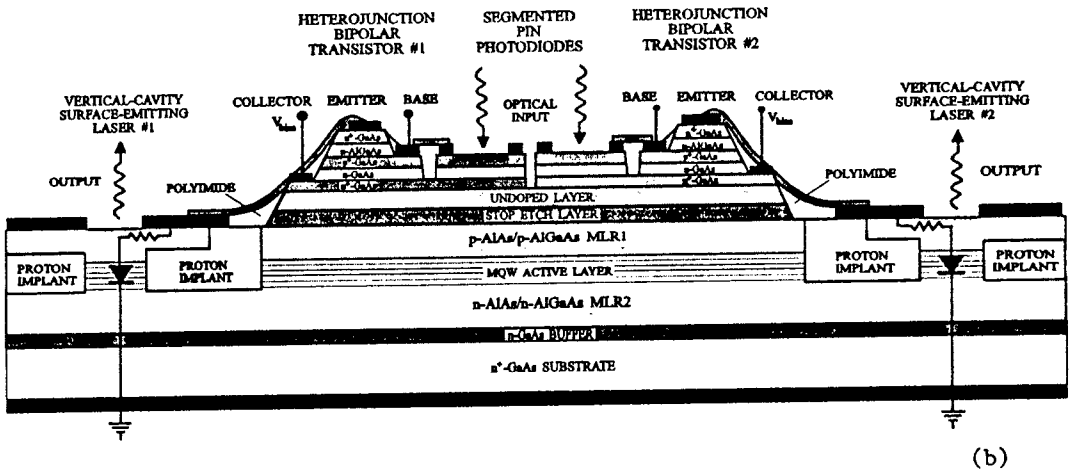
LARGE-SIGNAL MODULATION
200 MB/S EYE DIAGRAMS

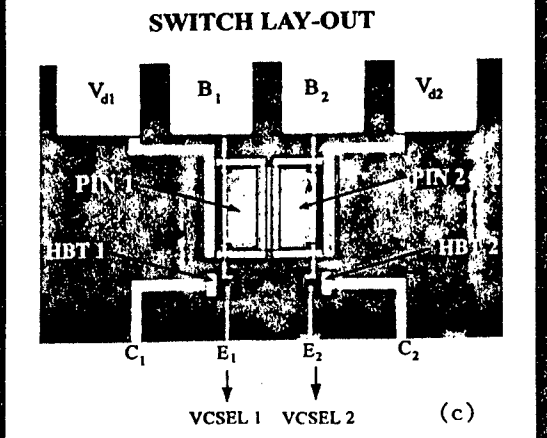
Fig 16

Julian Cheng
University of New Mexico, Center for High Technology Materials

INTEGRATED PIN/HBT/VCSEL OPTICAL ROUTING SWITCH







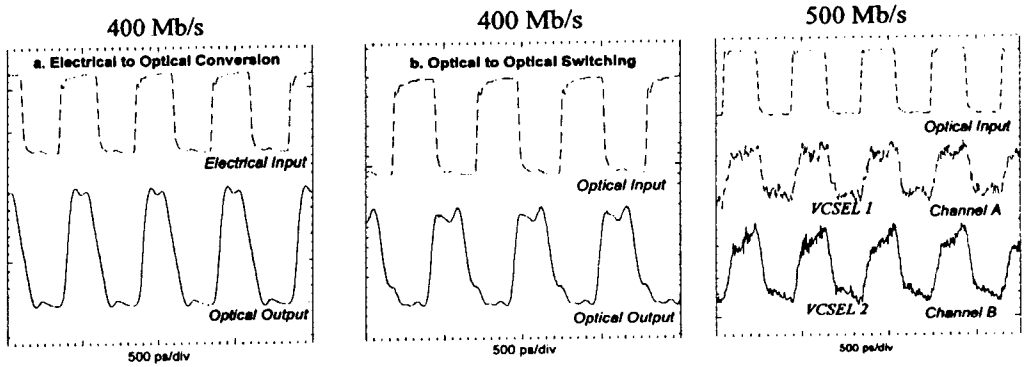


Fig 17

JULIAN CHENG
UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS

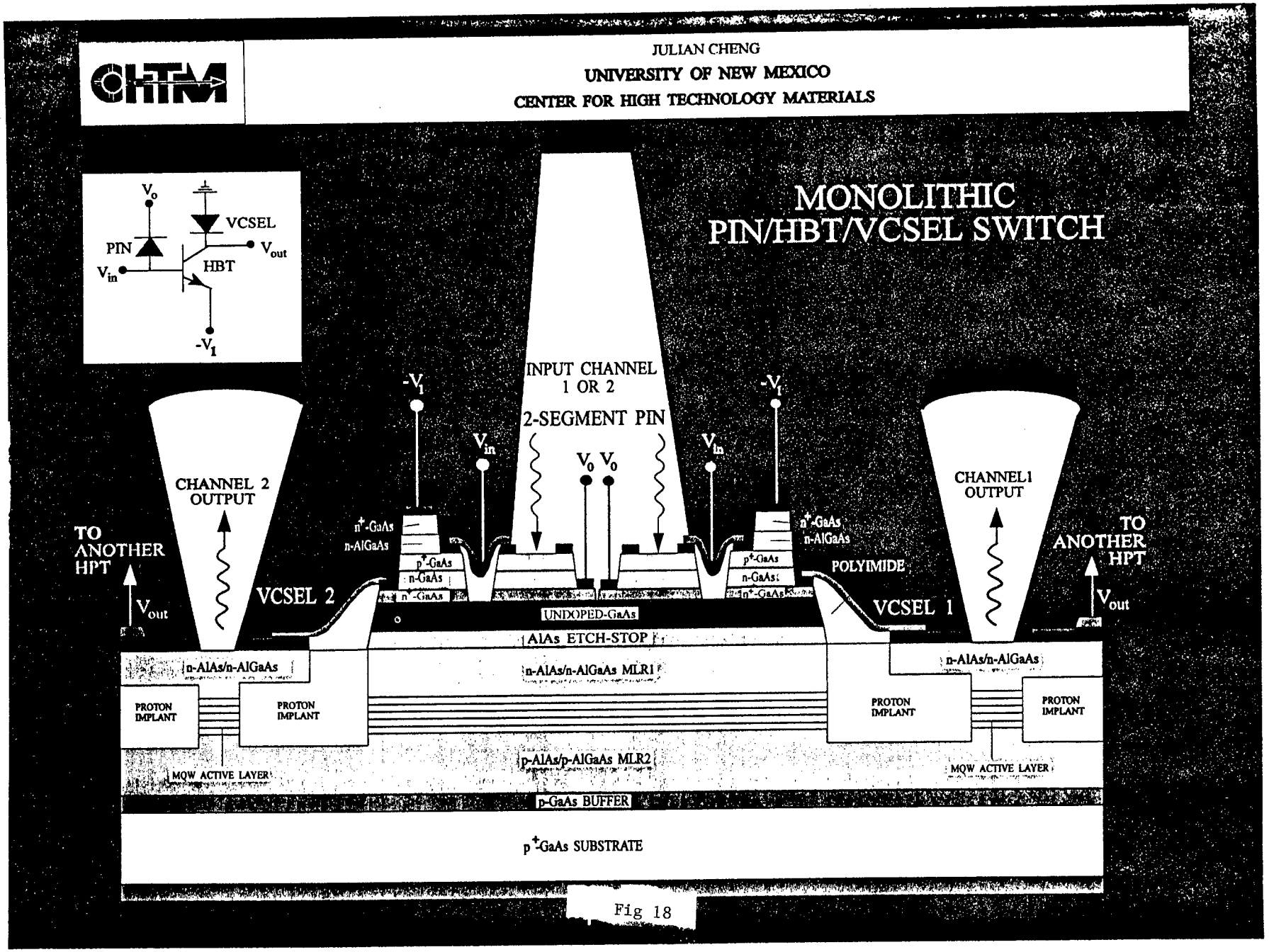
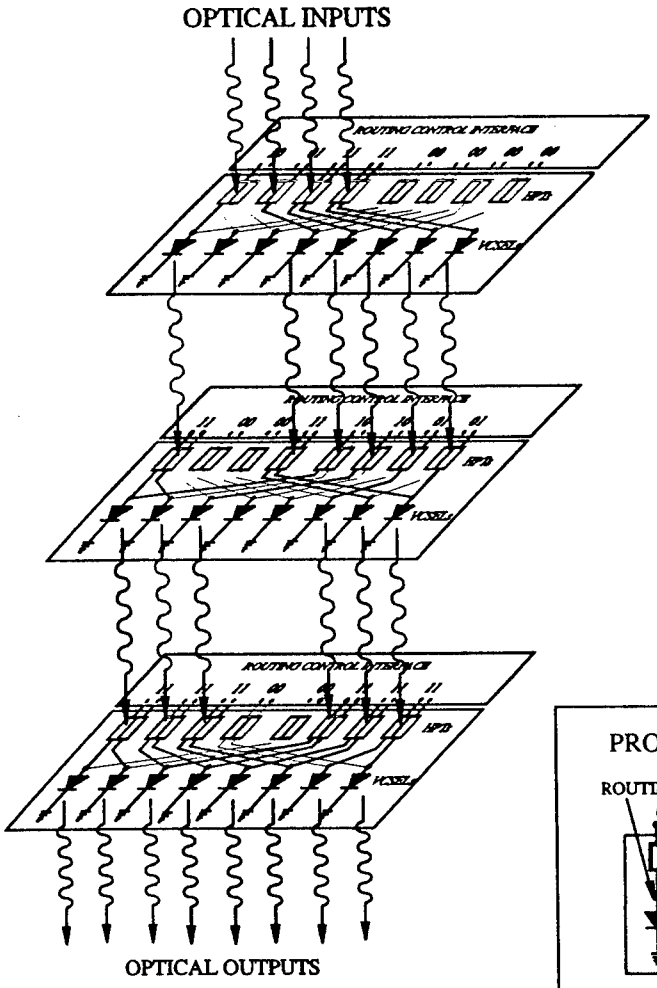


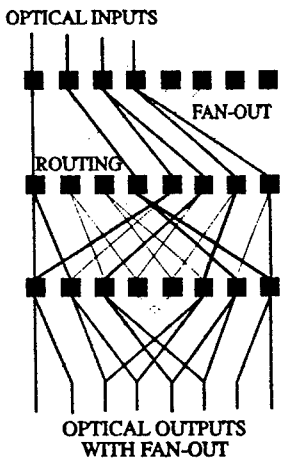
Fig 18

Fig 19

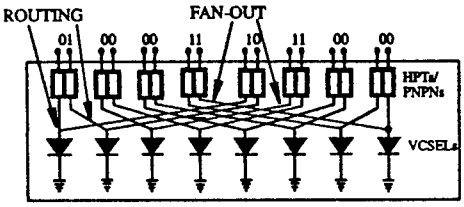
JULIAN CHENG
UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS

OPTICALLY CASCADED MULTI-STAGE SWITCH ARRAYS

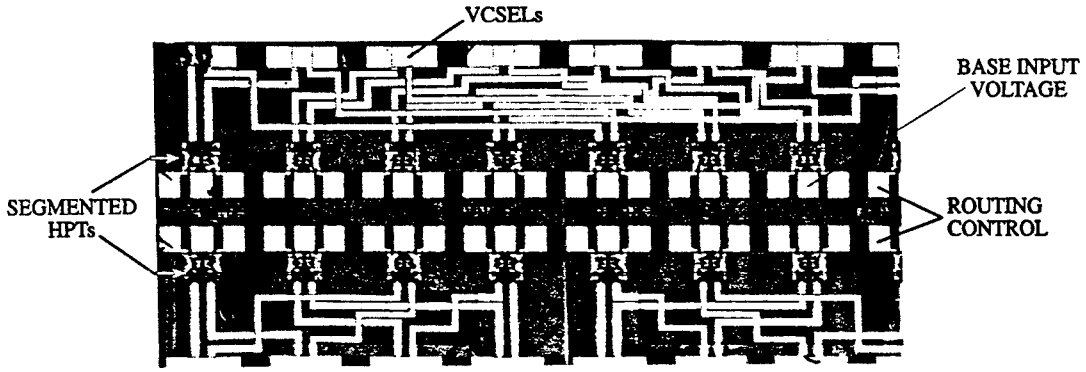




OPTICAL ROUTING NETWORK



RECONFIGURABLE 1x8 SWITCH ARRAY



JULIAN CHENG, UNM/CHTM

JULIAN CHENG
UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS

RECONFIGURABLE OPTICALLY-CASCADED MULTI-STAGE INTERCONNECT

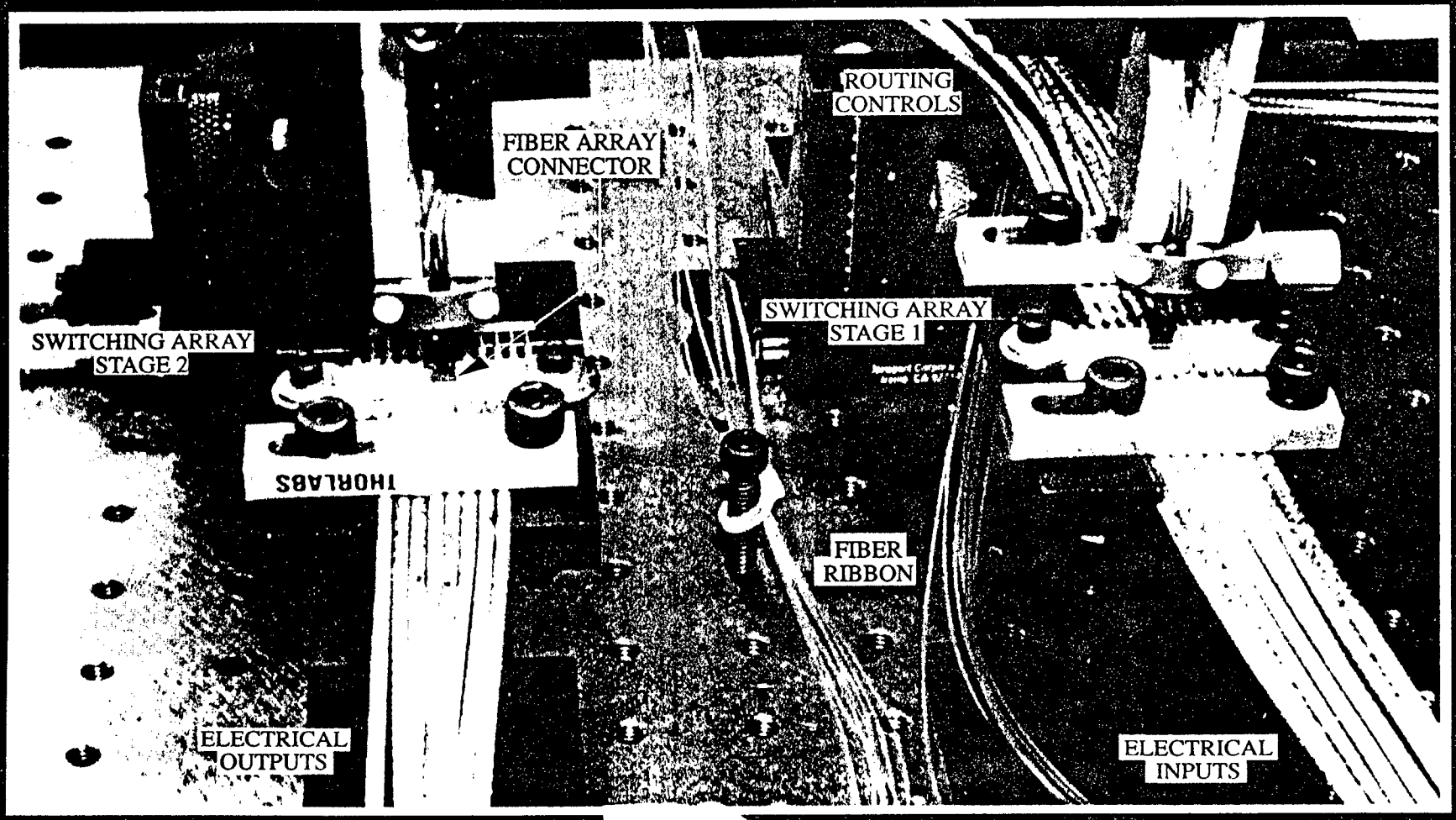


Fig 20

JULIAN CHENG
UNIVERSITY OF NEW MEXICO
CENTER FOR HIGH TECHNOLOGY MATERIALS

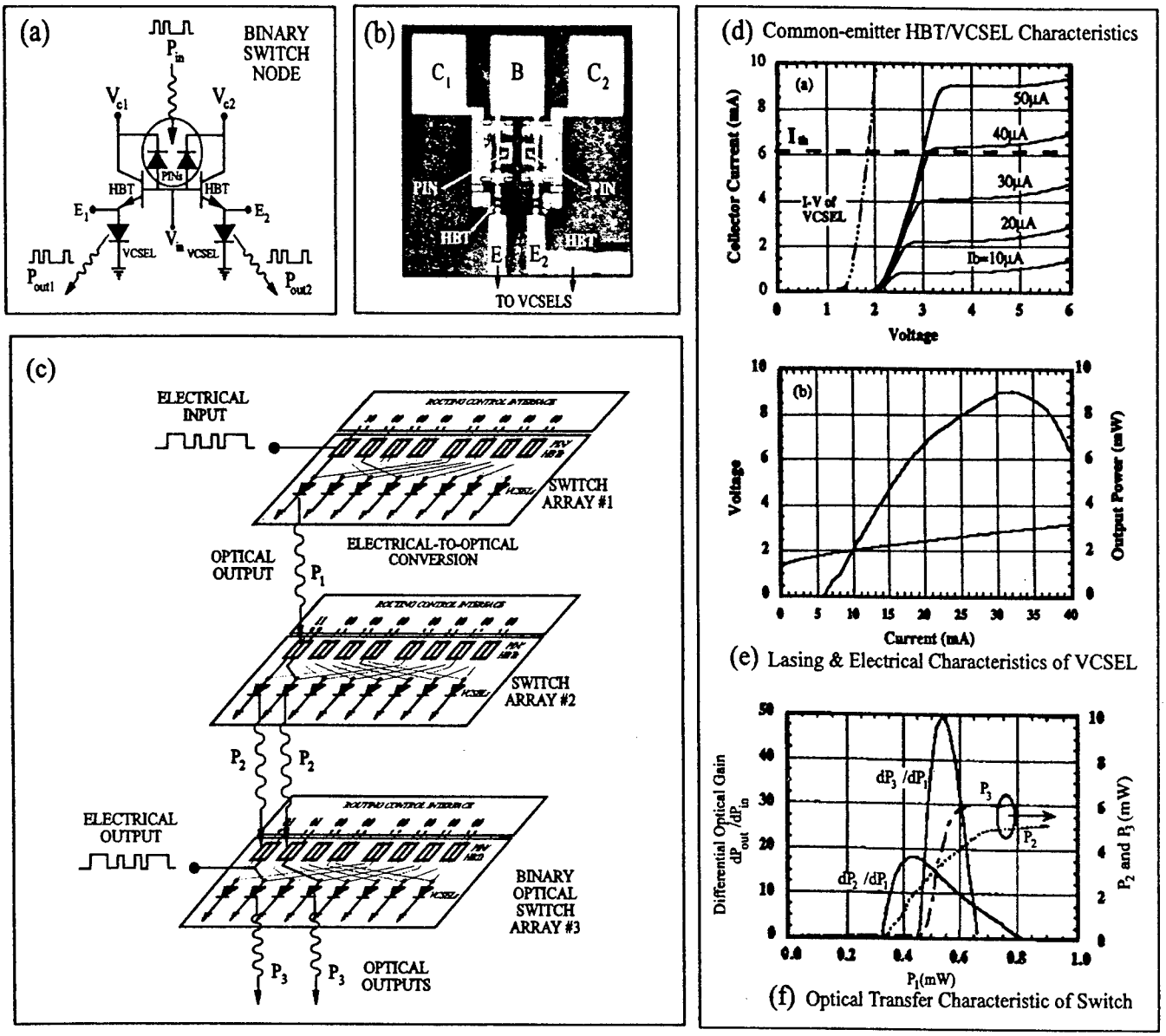


Figure . (a) The circuit design, and (b) layout of a reconfigurable binary PIN/HBT/VCSEL optical routing switch. (c) shows an optically-cascaded, multi-stage switching network using arrays of binary switches to perform optical routing functions. (d) shows the common-emitter characteristics of the HBT, (e) shows the lasing and electrical characteristics of the VCSEL, while (f) shows the differential optical gain of each of the two stages under optically cascaded dc switching operation.

Fig 21

•U.S. GOVERNMENT PRINTING OFFICE: 1997-509-127-47167

MISSION OF ROME LABORATORY

Mission. The mission of Rome Laboratory is to advance the science and technologies of command, control, communications and intelligence and to transition them into systems to meet customer needs. To achieve this, Rome Lab:

a. Conducts vigorous research, development and test programs in all applicable technologies;

b. Transitions technology to current and future systems to improve operational capability, readiness, and supportability;

c. Provides a full range of technical support to Air Force Material Command product centers and other Air Force organizations;

d. Promotes transfer of technology to the private sector;

e. Maintains leading edge technological expertise in the areas of surveillance, communications, command and control, intelligence, reliability science, electro-magnetic technology, photonics, signal processing, and computational science.

The thrust areas of technical competence include: Surveillance, Communications, Command and Control, Intelligence, Signal Processing, Computer Science and Technology, Electromagnetic Technology, Photonics and Reliability Sciences.